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System and Architecture Design of an NB-IoT RF Transceiver with a Polar Transmitter and On-chip Switching PA

Huimin Guo[1,2], Yuepeng Yan[1,2]

[1]*Institute of Microelectronics, Chinese Academy of Sciences, Beijing, China*
[2]*University of Chinese Academy of Sciences, Beijing, China*
E-mail: guohuimin.bj@gmail.com

Abstract. To develop low-power, low-cost Narrowband Internet-of-Things (NB-IoT) radio frequency (RF) transceiver chips, a novel hybrid polar transmitter architecture with an on-chip switching power amplifier (PA) is proposed. The transmitter consists of a hybrid supply modulator with a linear class-AB amplifier and a switching class-D amplifier for amplitude modulation. A two-point modulation frequency synthesizer is used for frequency modulation to achieve the error vector magnitude (EVM) and transmission spectrum optimization. Neither the receiver nor the transmitter requires an expensive surface acoustic wave (SAW) filter. The key parameters, such as the noise figure of the low-noise amplifier (LNA), phase noise and loop filter bandwidth of the frequency synthesizer, frequency step of the delta-sigma modulator and resolution of the digital-to-analog converter for the frequency modulation, are defined by the system-level simulation platform developed in the paper. Effects of the nonlinearity of the frequency-modulation varactor in the voltage-controlled oscillator (VCO) on EVM and transmission spectrum are also characterized. The architecture design and the system-level simulation provide a clear and quantifiable guidance to the circuit design of the NB-IoT RF transceiver.

Keywords: Narrowband Internet-of-Things, polar transmitter, two-point modulation, frequency synthesizer, radio frequency transceiver

Zasnova RF-sprejemno-oddajnega čipa s polarnim oddajnikom in preklopnim ojačevalnikom moči

Za razvoj nizkocenovnih in poceni radiofrekvenčnih (RF) sprejemno-oddajnih čipov na področju interneta stvari je v prispevku predlagana nova arhitektura hibridnega polarnega oddajnika s preklopnim ojačevalnikom moči. Oddajnik je sestavljen iz hibridnega napajalnega modulatorja z linearnim ojačevalnikom razreda AB in preklopnega ojačevalnika razreda D za amplitudno modulacijo. Ključni parametri, kot so šum, fazni šum in pasovna širina filtra zanke frekvenčnega sintetizatorja, frekvenčni korak modulatorja delta-sigma in ločljivost digitalno-analognega pretvornika za frekvenčno modulacijo, so določeni v postopku simulacije celotnega sistema. Opisani so tudi vplivi nelinearnosti v napetostno krmiljenem oscilatorju.

1 INTRODUCTION

Narrowband Internet-of-Things (NB-IoT) is a narrowband cellular communication technology standardized by The 3rd Generation Partnership Project (3GPP) with key requirements on the low-power and low-cost implementation for a long battery life and massive deployment [1-2]. Compared with the Long Term Evolution (LTE), NB-IoT scales down further in the cost and power consumption and coexists with the existing LTE infrastructure and spectrum. In the 3GPP Specification Release 13 and 14, NB-IoT is defined as a new category as "Category NB1" and "Category NB2", respectively, with the same requirements on the RF transceiver design. NB-IoT adopts a 180 kHz system bandwidth for both the downlink and uplink. For the downlink, the orthogonal frequency division multiple access (OFDMA) with a 15 kHz sub-carrier spacing and quadrature phase shift keying (QPSK) modulation are adopted. For the uplink, the single-carrier frequency division multiple access (SCFDMA) with a π/2-binary phase shift keying (BPSK) and π/4-QPSK modulation is used. The subcarrier spacing can be 15 kHz or 3.75 kHz, which is corresponding to 12 subcarriers or 48 subcarriers in a 180 kHz system bandwidth, respectively. Two types of the transmission, i.e., a single-tone transmission with a 3.75 kHz or 15 kHz subcarrier spacing and a multi-tone transmission with a 15kHz subcarrier spacing and 3, 6 or 12 subcarriers are supported. NB-IoT only supports the half-duplex operation.

As a new IoT connectivity technology, NB-IoT leverages the advantages of the cellular communication and narrowband communication. Although NB-IoT is defined as an evolution of LTE in the 3GPP specification, this new communication standard calls for different requirements on the terminal chip design,

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especially on the low-power and low-cost implementation. Since the NB-IoT specification was finalized by 3GPP in 2016, several system-on-chips (SoC) [3-4] and radio frequency (RF) transceivers [5-6] are reported. The on-chip power amplifier (PA) with a high average output power up to 23dBm is one of the key features to achieve the low-cost implementation, but it is also one of the main challenges of the NB-IoT RF transceiver design [7-8], which requires an in-depth study of both the architecture and circuit design. Although the on-chip PA is integrated in [3], the conventional direct up-conversion transmitter architecture is adopted, which leads to a higher power consumption due to the linear PA with a lower power efficiency. Off-chip PA are used in [4] and [5], which significantly increases the module cost and size. Advanced polar transmitter architecture with on-chip power amplifier is used in [6], but it can only support the single-tone transmission mode with a 3.75 kHz carrier spacing and cannot support the multi-tone transmission mode with a 15kHz carrier spacing for higher transmission data rate. Moreover, a detailed analysis on the transceiver system and architecture design or system-level simulation for the circuit parameter definition is not included in [3]-[6]. In the paper, the system and architecture design of an NB-IoT RF transceiver with a Surface Acoustic Wave (SAW)-less receiver and a hybrid polar transmitter with an on-chip switching PA is presented. The key system and circuit parameters are defined by the RF-baseband co-simulation based on a system-level simulation platform developed in the paper.

2 Receiver System Analysis and Architecture Design

2.1 Noise+interference budget allocation and IF selection

NB-IoT is a narrowband communication system, and a low-intermediate-frequency (low-IF) receiver is more suitable than a zero-IF receiver which is popular in the wideband communication system such as LTE. The receiver architecture is shown in Figure 1. To achieve a SAW-less receiver, a high linearity RF front-end is preferred. Therefore, a low noise amplifier (LNA) with a passive mixer and a 25%-duty-cycle local oscillator (LO) generation are adopted [9-10]. A complex filter is used as a channel selection filter (CSF) for the channel selection and image rejection. A programmable gain amplifier (PGA) with the gain step of 1dB is adopted for the gain control by the digital baseband. A 10-bit asynchronous successive-approximation-register analog-to-digital converter (SAR-ADC) [11-13] samples the IF signal centered at 480 kHz with a 15.36 MHz sampling clock, followed by a decimation filter to down-sample the IF signal to 1.92 MHz and increase the digital output bit-width to 12bits to relax the requirement on both the CSF out-of-band attenuation and ADC resolution.

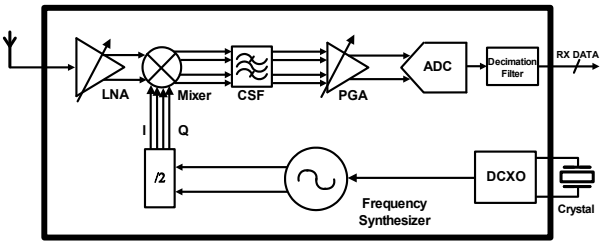


Figure 1. Low-IF receiver architecture.

The receiver sensitivity (*Ps*) requirement defined in the 3GPP specification for the NB-IoT downlink is -108.2dBm. The noise bandwidth (*BW*) is the same as the system bandwidth, i.e., 180 kHz. The implementation margin (*IM*) is the same as that of LTE, i.e., 2.5 dB, and the SNR requirement for demodulation is usually less than 2dB. According to (1), the total noise+inteference (*N+I*) budget is around 9dB.

$$P_S = -174dBm/Hz + 10\log(BW) + SNR + IM + (N+I) \quad (1)$$

In the NB-IoT RF transceiver, there is no transmitter signal leakage to receiver thanks to the half-duplex operation. The SAW-less receiver also eliminates the insertion loss contributed by the SAW filter. Therefore, the noise figure (NF) budget of the NB-IoT receiver can be larger than that of the LTE receiver supporting the full-duplex operation. Assuming the total insertion loss of the printed circuit board (PCB) trace is 1dB, there is an 8dB (N+I) budget left for the receiver. Since the out-of-band (OOB) blocking requirement is very stringent for the SAW-less receiver with a small filtering function at the RF front-end, it is reasonable to allocate 6dB budget to NF to reduce the LNA/mixer current consumption and 2dB budget to nonlinearity to relax the LNA/mixer linearity requirement.

The intermediate frequency (IF) selection in a low-IF receiver should balance the image rejection requirement and ADC capability properly. Since the number of the cyclic prefix (CP) defined in the 3GPP specification is 144 or 160 for the sample rate of 30.72 MHz, the clock to baseband for the data transmission is usually set to 1.92 MHz to keep the number of CP as an integer, i.e., 9 or 10. Theoretically, IF should be lower than 860 kHz to avoid aliasing during the ADC sampling. In this design, IF is selected as 480 kHz to mitigate the flicker noise from the transistors with a sufficient image rejection.

2.2 Out-of-band blocking consideration

The OOB blocking is a critical requirement on the SAW-less receiver design. There are mainly two considerations of the OOB blocking requirement, i.e., the LO phase noise and RF front-end nonlinearity. The LO phase noise requirement comes from the reciprocal

mixing of the interferer with the phase noise at the frequency of the interferer location ± IF. The mixed product that appears in the IF signal channel decreases the effective SNR. A more stringent OOB blocking requirement leads to a lower LO phase noise requirement, thus a higher current consumption.

A strong interferer decreases the effective gain of the RF front-end and leads to a larger effective NF and a lower SNR. With no SAW filter, the LNA gain should be decreased to improve the linearity when strong interferer exists to pass the most stringent OOB blocking requirement of -15dBm at +/-150MHz offset for the low band (LB) and -15dBm at +/-200MHz for the high band (HB). However, as shown in Figure 2, since the OOB interferer location is beyond the signal frequency band, it is filtered by CSF and cannot be detected by the digital modem.

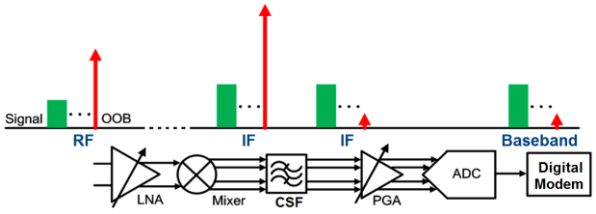


Figure 2. Illustration of the OOB interferer filtered by CSF.

In this design, an automatic gain control (AGC) is developed to detect the interferer automatically to increase the RF front-end linearity, which is shown in Figure 3. Two identical analog received signal-strength indicator (RSSI) modules with two identical 8-bit ADCs are used to detect the interferer at the RF front-end input. With the presence of the interferer, the two RSSI modules will detect different IF power levels and there will be a difference between the two ADC output codes. Therefore, the digital baseband can utilize this information to decrease the LNA gain properly, thus increasing the linearity of the RF front-end.

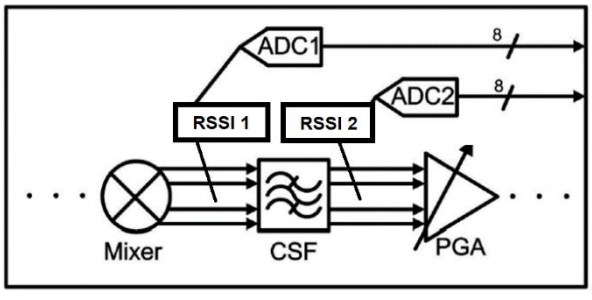


Figure 3. Proposed AGC architecture.

A system-level simulation platform based on the Keysight's SystemVue simulation tool is developed to verify the system and module parameter definition. A low-IF receiver shown in Figure 1 is modelled. The key parameters of the receiver including the LNA NF and nonlinearity, the phase noise of the frequency synthesizer and the ADC resolution are properly defined by evaluating the effects of these parameters on the receiver block error rate (BLER). Table 1 shows the key parameters of the modules in the receiver defined by the system-level simulation.

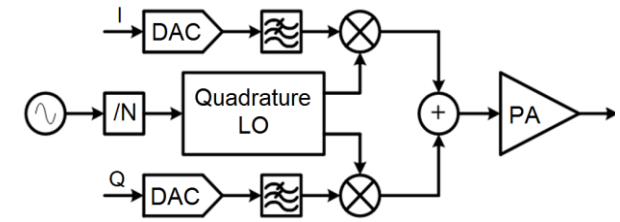
Table 1. Receiver key parameters definition.

Module	Key parameters	
Low-noise Amplifier	Noise Figure<4.5dB	Output 1dB Compression Point>-4dBm
Mixer	Flicker Noise Corner<100kHz	Maximum DC Offset<20mV
Channel Selection Filter	-3dB Bandwidth=300kHz	Image Rejection>30dB
Programmable Gain Amplifier	Gain Tuning Range =10-60dB	Gain Step=1dB
Analog-to-Digital Converter	Resolution=10bits	Sampling Rate=15.36MHz
Frequency Synthesizer	Integrated Noise<2 degrees	Phase Noise @200kHz offset<-95dBc/Hz @1MHz offset<-120dBc/Hz @10MHz offset<-137dBc/Hz

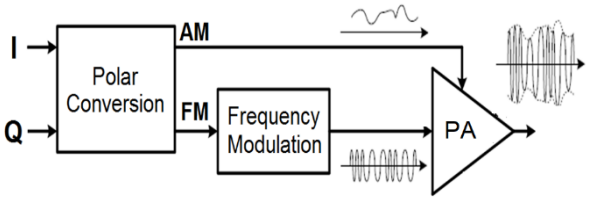
3 TRANSMITTER SYSTEM ANALYSIS AND ARCHITECTURE DESIGN

3.1 Transmitter architecture selection

The direct up-conversion transmitter and polar transmitter are two popular transmitter architectures in the RF transceivers. As shown in Figure 4, the direct up-conversion transmitter can process the wideband modulation signal up to tens of MHz, but it requires a linear PA with a lower power efficiency. The average output power is limited if an on-chip PA is used in the direct up-conversion transmitter. Therefore, an off-chip PA is usually used which leads to a higher cost and a larger module size. Moreover, the direct up-conversion transmitter requires a complex calibration circuit to eliminate the carrier leakage and I/Q gain/phase imbalance. The polar transmitter converts the I/Q data into the amplitude modulation (AM) data and the frequency modulation (FM) data and modulates the amplitude in PA and frequency in the frequency synthesizer, respectively. It is suitable for narrowband modulation and the on-chip switching PA with a high power efficiency can be used for a high output power. The carrier leakage and I/Q gain/phase imbalance are intrinsically negligible with no up-mixing operation. However, there are several technical challenges, such as the AM to AM distortion, AM to FM distortion and AM to FM timing mismatching calibration in the polar transmitter design.



a) Direct up-conversion transmitter



b) Polar transmitter

Figure 4. Transmitter architecture comparison.

The NB-IoT applications are usually cost-sensitive, so the off-chip PA is highly demanded to be removed. Moreover, since there is a 5-6dB peak-to-average power ratio (PAPR) in the NB-IoT multi-tone signal, the power efficiency is very low if a linear PA is used. In this design, the polar transmitter with on-chip switching PA is adopted for a high-integration and low-power design. The low transmission noise can be achieved with the polar transmitter by avoiding using the up-conversion mixer, thus the commonly used SAW filter at the transmitter output can be eliminated. As shown in Figure 5, the 11-bit I/Q baseband data are converted to the AM and phase modulation (PM) data by a coordinate rotation digital computer (CORDIC) module. Then the 27-bit PM data and 9-bit AM data are passed into a look-up table (LUT) for a digital pre-distortion followed by the PM to FM conversion. After the AM and FM path timing alignment, the FM data are passed into the frequency synthesizer and the AM data are up-sampled and passed into a 9-bit digital-to-analog converter (TX_DAC) followed by an image rejection filter (TX_LPF) for amplitude modulation. One buck-boost DC-DC converter is dedicatedly used to supply the on-chip switching PA via the hybrid supply modulator which consists of a linear Class-AB amplifier and a switching Class-D amplifier.

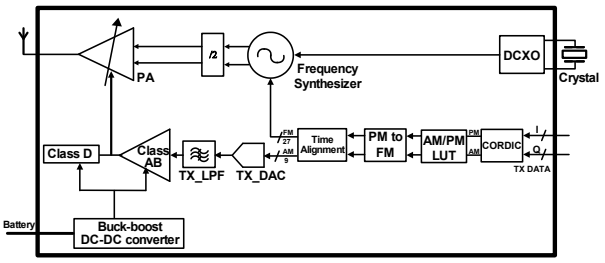


Figure 5. Polar transmitter architecture.

3.2 Hybrid supply modulator and digital pre-distortion

There are two types of the polar transmitter, i.e., the analog polar transmitter and the digital polar transmitter. The analog polar transmitter converts the AM data to an analog signal by TX_DAC and TX_LPF and uses the supply modulator to modulate the PA power supply for the amplitude modulation. In the analog polar transmitter, the switching PA always works at the saturation region to achieve the highest power efficiency. The digital polar transmitter modulates the switching PA cell directly for the amplitude modulation. The digital polar transmitter is simpler than the analog polar transmitter, but it suffers from the sampling image in the digital-to-RF conversion which may cause spurs at the sampling frequency offset in the transmission spectrum. Usually, in the digital polar transmitter, the AM data are up-sampled to a higher frequency to mitigate the sampling image effect. Moreover, with a constant power supply, the switching PA does not always work in the saturation region, thus the PA power efficiency is not always optimized in the digital polar transmitter [14-15].

To leverage the advantage of both the analog polar transmitter and the digital polar transmitter, a hybrid polar transmitter architecture is proposed. As shown in Figure 6, the Class-AB amplifier modulates the power supply of the PA together with the Class-D amplifier via an off-chip inductor. For an average output power-level higher than 10dBm (high-power mode), an analog polar transmitter is used and the AM data are input into the Class-AB amplifier. The Class-AB amplifier provides a small modulation current while the Class-D amplifier provides a large DC current to supply PA. Both AM and power-level control are implemented in the Class-AB amplifier (as shown by a red line in Figure 6). In the high-power mode, the voltage ripple at the Class-AB amplifier output must be less than 20mVpp to meet the spectrum emission mask (SEM) requirement and the spurious emission limit. For an average output power level lower than 10dBm (low-power mode), PA works in the digital polar transmitter mode. The Class-AB amplifier is bypassed from its power supply to the output and the Class-D amplifier is turned off. AM is achieved by a direct on/off modulation in the switching PA cells and the power-level control is achieved by adjusting the PA supply voltage (as shown by the blue line in Figure 6). A buck-boost DC-DC converter which can provide output voltage as low as 312.5mV with the tuning step of 12.5mV is used as the PA power supply for an accurate output power-level control. The digital polar transmitter can be used in the low-power mode because the power efficiency and the spurious emission are not so critical in the low-power mode as they are in the high-power mode. Therefore, with the hybrid polar

transmitter, the power efficiency and transmitter performance are optimized simultaneously in both the high-power and low-power mode.

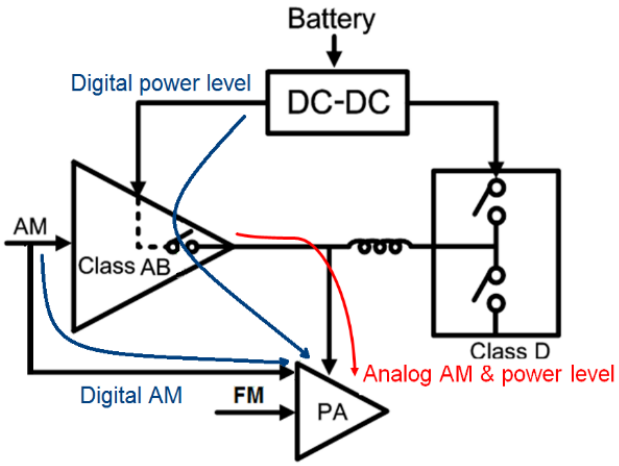


Figure 6. Hybrid polar transmitter.

For both the analog polar and digital polar transmitter, the digital pre-distortion is necessary since the relationship between the output power of the switching PA and its power-supply voltage is intrinsically nonlinear. The digital pre-distortion is designed by LUT stored in the memory of the chip. There are totally 16 LUTs corresponding to 64 different power levels to save the total LUT size. Each table has 9bits for the AM-AM predistortion mapping and 7bits for the AM-PM predistortion mapping. LUT is measured in the laboratory when the RF transceiver works in the calibration mode. The 9-bit power control codes are input externally, and the power of the PA output sinewave signal is measured accordingly. After obtaining the nonlinear relationship of the PA output power versus 9-bit power-control codes, LUT can be formed to achieve the linear relationship after compensation. In the high-power mode, since the 9-bit power-level control codes are input from TX_DAC, the nonideal effect of TX_DAC, TX_LPF, Class-AB amplifier and PA are all characterized in the digital pre-distortion. In the low-power mode, only the nonideal effect of PA is necessary to be characterized.

3.3 Two-point modulation frequency synthesizer

After I/Q to AM/PM conversion and PM to FM conversion, the signal bandwidths of both the AM and FM data are extended to several times of the original I/Q signal bandwidth. Therefore, in the single-point modulation, the bandwidth of the FM data is limited by the frequency synthesizer loop-filter bandwidth. A better Error Vector Magnitude (EVM) can be achieved with a larger loop filter bandwidth since less high-frequency FM data are filtered. However, it will induce more noise from the delta-sigma modulator to the frequency synthesizer output, thus degrading the transmission spectrum. This is an intrinsic contradiction in the single-point modulation. Therefore, the two-point modulation frequency synthesizer is adopted in this design to enable a larger bandwidth frequency modulation with a narrower frequency synthesizer loop-filter bandwidth. The narrower bandwidth also leads to a better phase noise, thus a better transmission spectrum. As shown in Figure 7, the FM data are separated into a low-frequency (LF) path for the delta-sigma modulator modulation and a high-frequency (HF) path for the VCO modulation. For the LF path, since NB-IoT requires to support the 3.75kHz single-tone modulation, the 27-bit delta-sigma modulation is adopted to achieve a 0.57Hz frequency resolution. For the HF path, a 12-bit current-steering DAC followed by a differential-to-single-ended conversion buffer converts the FM data to an analog voltage to control the FM varactor array in VCO. The DAC resolution is defined by the system-level simulation with a consideration of the tradeoff between EVM and the DAC area and current consumption. Only the first 12-bits (i.e., MSB to MSB-11) of the 27-bit FM data are input into DAC for the HF path frequency modulation. A gain calibration with a 7-bit control for DAC is designed to tune the gain mismatch between the LF and HF path to achieve less than 5% of the frequency error. The timing mismatch can be adjusted in either the HF or the LF path by the delay adjustment module before the FM data are input into DAC or the delta-sigma modulator. With the two-point modulation, the frequency synthesizer bandwidth can be set narrower to achieve the performance optimization for both EVM and transmission spectrum.

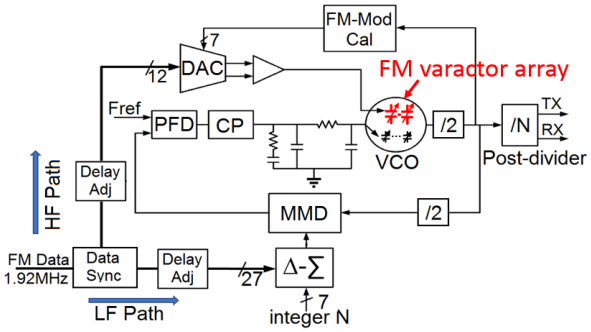


Figure 7. Two-point modulation frequency synthesizer.

As shown in Figure 8, the LC tank VCO with an NMOS tail current source is used. The FM varactor array is paralleled with the switch cap array for the PLL locking. The DAC output is used to control the FM varactor for the frequency modulation. The effect of the FM varactor nonlinearity on EVM and transmission spectrum is simulated quantitively by the system-level platform developed with the SystemVue simulation tool. The relationship between the VCO frequency and the control voltage of the FM varactor is achieved in the circuit-level simulation and is fit into a polynomial function used in the system-level simulation to characterize the effect of the FM varactor nonlinearity on EVM and transmission spectrum. The simulation result is shown

in Figure 9. Without the varactor nonlinearity, the spectrum for the multi-tone transmission is nearly ideal and EVM is 1%. With the varactor nonlinearity, the spectrum is degraded but it still meets the SEM requirement and EVM is degraded to 3%. Therefore, the system-level simulation provides a clear and quantitative guidance to the circuit parameter definition and design.

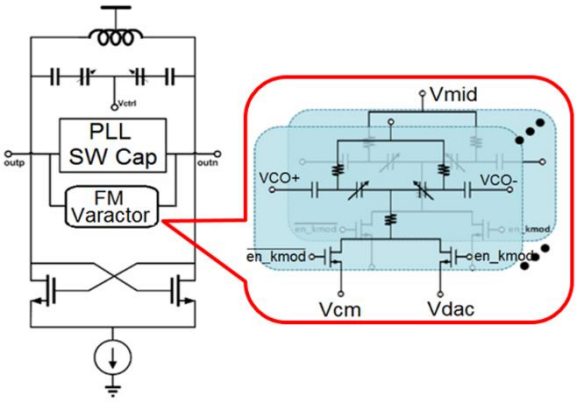


Figure 8. VCO architecture and FM varactor array.

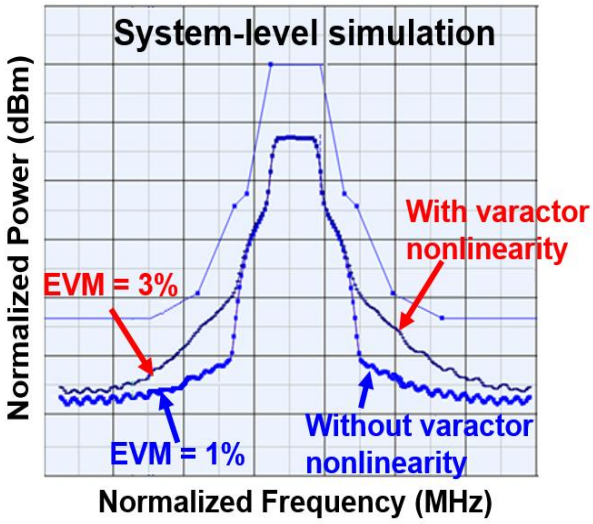


Figure 9. System-level simulation for the effect of the varactor nonlinearity on EVM and transmission spectrum.

The key parameters to evaluate the NB-IoT transmitter performance include EVM, SEM, adjacent channel leakage rejection (ACLR) and spurious emission. EVM, SEM and ACLR are mainly related to the linearity of the transmitter and modulation quality. The spurious emission is related to the transmitter architecture and frequency synthesizer design. Other key parameters, such as the carrier leakage and I/Q gain/phase imbalance, are negligible thanks to the polar transmitter architecture. Table 2 shows the key parameters in the transmitter defined by the system-level simulation.

Table 2. Transmitter key parameters definition.

Module	Key parameters	
Power Amplifer	Control Bitwidth=9bits	Maximum Output Power=27dBm
Delta-sigma Modulator	Resolution=27bits	Frequency Step=0.57Hz
Digital-to-Analog Converter for FM	Resolution=12bits	Sampling Rate=38.4MHz
Frequency Synthesizer	Loop Filter Bandwidth<150kHz	Phase Noise @200kHz offset<-95dBc/Hz @1MHz offset<-120dBc/Hz @10MHz offset<-137dBc/Hz

4 Conclusion

The paper presents a system and architecture design of a SAW-less NB-IoT RF transceiver with a hybrid polar transmitter and on-chip switching PA. A two-point modulation frequency synthesizer architecture is developed to optimize both EVM and transmission spectrum. An AGC architecture is designed to detect the OOB interferer and increase the RF front-end linearity automatically for the SAW-less receiver. The key system and module parameters are defined and nonideal effects of the key components are characterized by the system-level simulation. The NB-IoT RF transceiver chip based on the architecture design and parameter definition is successfully developed [16].

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Huimin Guo received his B.Sc. degree and M.Sc. degree in physics from Beijing Normal University in 2000 and 2003, respectively. He is currently working towards his Ph.D. degree at the Institute of Microelectronics, Chinese Academy of Sciences in China. His research interest is in analog circuit design and RF transceiver system and circuit design. He is an IEEE Senior Member.

Yuepeng Yan received his Ph.D. degree in information and systems sciences from Ibaraki University, Japan. Currently he is a professor at Institute of Microelectronics, Chinese Academy of Sciences in China. His research interest is in integrated circuit design and system-on-chip (SoC) design.