ELEKTROTEHNIŠKI VESTNIK 78(4): 198-204, 2011
ENGLISH EDITION

A Controlled High-Voltage DC Source for Power Semiconductor Components Testing

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Abstract: The presented high-voltage DC source was designed to enable laboratory measurements of reverse and forward characteristics in non-conducting state of power semiconductor components. It also enables to measure the minimum triggering current or control voltage in dependence of the voltage on main electrodes for SCR, triac or voltage-controlled semiconductor devices such as MOSFET and IGBT, respectively. The source consists of a high-voltage switching converter, voltage and current measuring subsystems and electrically insulated linear-mode current source. Control and measuring tasks inside the source are performed by means of an 8-bit Microchip microcontroller 18F452. The switching converter is comprised of a flyback step-up transformer and four identical secondary modules connected in series. The flyback transformer is carefully constructed to minimize its stray capacitance and leakage inductance. These parasitic components cause high-frequency oscillations and make setting of the precise output voltage even more difficult. In proposed aiming of improving the output-voltage control, the turn-on speed of the switching MOSFET is decreased and, consequently, the charging current of the transformer parasitic capacitors is limited.

Keywords: Flyback switching converter, MOSFET, High-voltage transformer, High-frequency oscillations, Reverse current.

1 INTRODUCTION

It is usually assumed that new power semiconductors are faultless and that their features comply with the specifications declared in datasheets. How true these presumptions are depends on the manufacture quality and the final quality tests at the manufacturer. For example, when constructing a prototype device to be used for medical [1], military or aerospace purposes, each power semiconductor should be tested in order to assure high performance reliability of the device. Power semiconductor components should also be tested in any case of the device malfunctioning. The aim of the paper is to describe a concept of a laboratory prototype of the high-voltage DC source, in contrast to the pulse bipolar source [1], with the nominal output voltage of 2 kV and the current capability of 2 mA. The proposed concept can be easily adapted to a source of higher nominal values.

2 CONCEPT OF THE HIGH VOLTAGE SOURCE

In order to generate high voltage at the source output, it is of vital importance to select and design a "power" converter meeting our expectations. In past, we used a laboratory source consisting of a cascade multiplier with a variac at its input. Such simple concept enabled no digital control. A logical choice is a switch-mode converter, driven by a microcontroller using a PWM digital output.

The overall block diagram of our high-voltage DC source is presented in Fig. 1. For the control and measuring purposes an 8-bit Microchip microcontroller 18F452 is used. It has two output PWM channels, initialized for 10-bit resolution and consequently running at 39 kHz. Of the eight available input channels of a 10-bit ADC module, six were used in our application. Three channels were used to measure the process quantities and the other three were inputs of the reference values. The switching converter was controlled by the first PWM signal with its duty cycle limited to 0.5 and the reference for the output voltage set by potentiometer U_{ref}. The device under test (DUT) was at the converter output with a subsystem enabling differential-voltage measurement connected in parallel and with a subsystem for the main-current measurement connected in series. The maximum current through the tested component can be limited by setting the potentiometer for I_{LIM}. An additional linear-mode electrically-insulated current source of the nominal value of the output current equal to 100 mA was designed in order to measure the dependence of the minimum triggering current on the preset voltage in static states on the main electrodes for SCR or triac. The current source was controlled by the second PWM channel by means of the reference value $I_{G,ref}$ on the channel AD5. The PWM signal with a fully variable

Received October 24, 2011
Accepted November 7, 2011

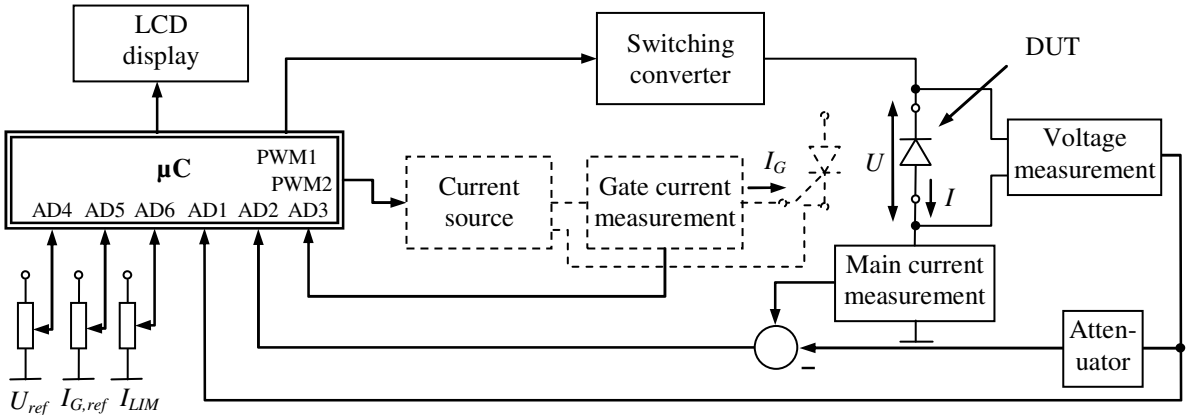

Figure 1. Block diagram of the proposed high-voltage DC source

duty cycle was led through an opto-coupler and then filtered with a low-pass filter to obtain the control voltage for the voltage-controlled current source (Fig. 2). If the gate and emitter (or the source) of the voltage-controlled components under test are bypassed by resistor R_B of 100 Ω, the gate voltage of up to 10 V can be preset. In this way the gate threshold voltages of MOSFETs and IGBTs can be measured. Instant values of the measured quantities are displayed on a four-row display together with duty cycles of the corresponding PWM channels (Fig. 12).

3 TOPOLOGY OF MEASURING SUBSYSTEMS OF THE HIGH-VOLTAGE SOURCE

Each of the three measuring subsystems is designed to give 5 V on the output at the maximum value of the measured quantity. This is the ADC voltage range in the µC. The topology of the measuring subsystems and of the electrically insulated current source is shown in Fig. 2. Besides the voltage divider, current shunts were also designed to obtain the nominal value of 5 V. Consequently the required gains of the instrumentation amplifiers are equal to one and interferences in the measured signals are not amplified. Because of the relatively small value of measured current I flowing through DUT, superimposed current I_U through R_I, which is a consequence of the current through the voltage divider resistors R_{U1}, R_{U2}, can not be neglected. This is why the scaled value of the measured signal of the source output voltage is subtracted from the voltage drop at current shunt R_I and thus correct information of the current through DUT is obtained.

4 TOPOLOGY OF THE HIGH-VOLTAGE CONVERTER

Topology of the high-voltage converter is shown in Fig 3. Its central part is a ferrite switching transformer [2] with four secondary windings. The concept for the topology on the secondary side was modular in order to mitigate the requirements for the transformer inner insulation and to use lower voltage components with regard to the relatively high output voltage. So, there are four rectifiers with corresponding filter capacitors with their outputs connected in series, one for each separated winding. When the PWM duty cycle controlling the switching MOSFET is set to maximum (0.5), the mean value of the rectified voltage is between 500 V to 800 V on each module. The value of this voltage is low if the source output terminals are short-circuited and only protective resistor R_P is loading the converter. The highest voltage would occur without varistors and no

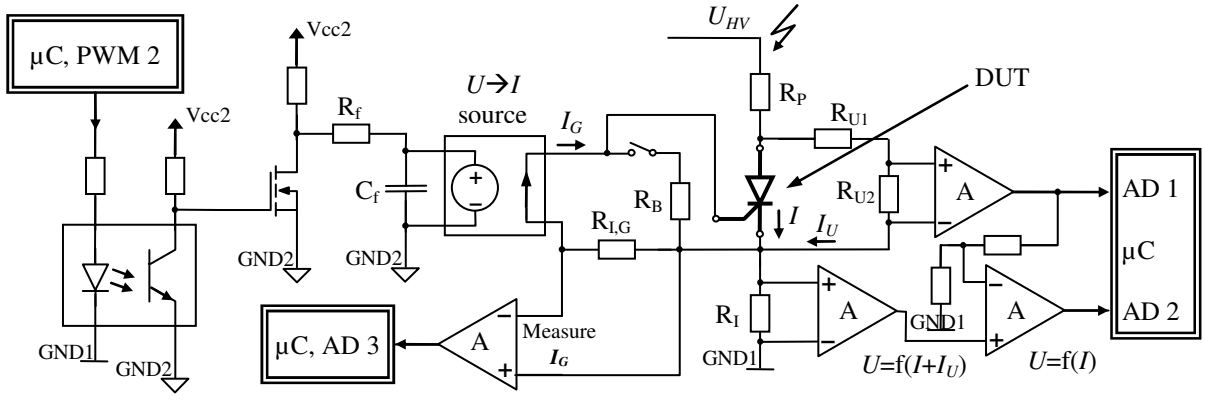

Figure 2. Topology of the measuring units used for the proposed high-voltage source

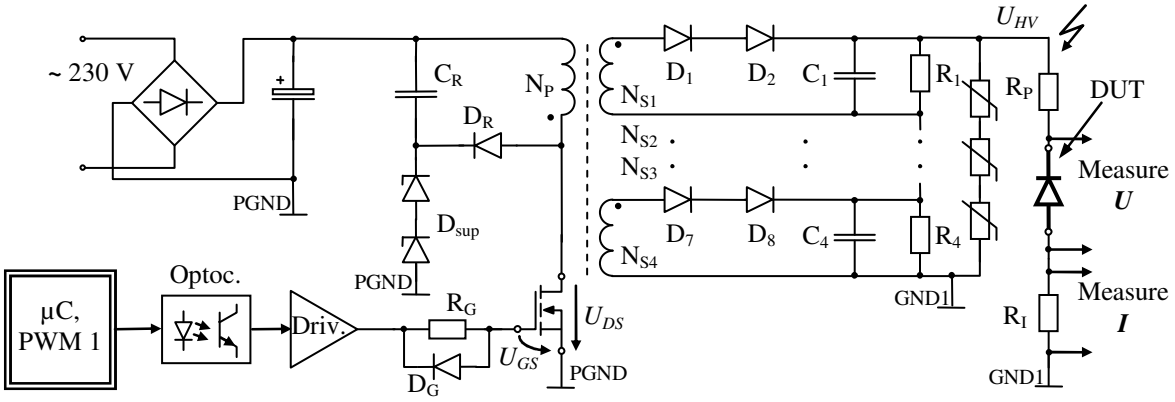

Figure 3. Topology of the flyback switching converter with the high-voltage output

load on the output terminals. Varistors that were added to the converter output protected its components by limiting the maximum voltage and consequently protected also the measuring ADC from excessive overloading. In the performed design measures, inexpensive 1000 V/1 A ultra-fast rectifier diodes were used. To prevent the negative voltage on the transformer secondary from exceeding their peak reverse voltage at a high output voltage, two diodes were connected in series.

4.1 Principle of Precise Output-Voltage Setting

In the first iteration of the source design, a fly-back converter was implemented because of its simple output topology. In testing the source prototype we found it difficult to determine precise low-voltage set points. It was almost impossible to set voltages lower than 1000 V. To solve the problem, a forward topology [3, 4] of the switching converter was implemented and tested for a certain period of time. However, experiments performed with this topology gave rise to difficulties in terms of the precise output-voltage control. After identifying the real cause of the problem and studying the most suitable topology for the low-power applications, the flyback topology was successfully implemented. This time the flyback transformer was finally designed in the way minimizing the stray capacitance and leakage inductance.

The idea of precise output voltage setting within the whole range relies on shifting the precisely allotted energy packages from the input supply to the output circuit by means of the flyback transformer. Theoretically, these energy packages are during the MOSFET on-time transferred into the transformer which in the flyback topology acts like a storage inductor. By controlling the peak value of the primary current, the precise energy packages stored in the core magnetic field are

$$W_m = \frac{1}{2} L I^2 . \quad (1)$$

After the MOSFET turns off, this energy is transferred into the secondary side. In the case of the converter open-loop control, a certain duty cycle is needed for a given output current and voltage. If no load is connected to the output, a parallel current path should be provided to preset the desired output voltage. This path goes through bleeder resistors R_1 to R_4 on the output of the secondary modules (Fig. 3) in parallel with voltage divider resistors R_{U1} and R_{U2} (Fig. 2). The maximum output voltage is usually limited by a voltage clamp (D_{sup} for example), or, in our case by varistors.

Precisely controlled energy transfer can only be maintained by a transformer having no stray capacitances. In practice, though capacitances can be minimized, there is no way of completely avoiding them. Consequently, energy transfer is not performed only by energy packages stored in the inductor but also by energy packages stored in parasitic capacitors. The problem with the latter packages is that they can not be controlled by the duty cycle. The capacitor is charged soon after the MOSFET is turned on. The only way to control the energy packages in a parasitic capacitor is to control the charging speed by limiting the charging current. An additional series resistor is not a solution since it would produce excessive additional losses at higher loads. The optimal solution is to decrease the MOSFET turn-on speed. By optimizing the time of the linear mode of the MOSFET operation, the converter efficiency is not impaired because of suppressed high-frequency oscillations and minimized EMI. On the other hand, the inductor magnetizing current does not increase considerably when MOSFET is already through its operating in linear mode. The speed of MOSFET turning on is decreased by using gate resistor R_G (Fig. 3). Its resistance value is some 100-times higher than the one of other switch-mode applications.

4.2 Transformer High-Frequency Equivalent Circuit

To obtain a satisfactory model for high-voltage high-frequency performance, the usual equivalent circuit for a two-winding transformer needs to be upgraded with parasitic capacitors. Such simplified equivalent circuit is depicted in Fig. 4a [5]. Winding resistances resistors,

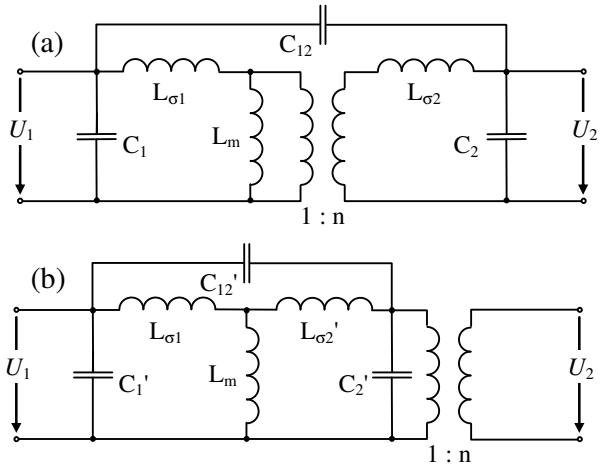

Figure 4. Equivalent circuit of a two-winding high-frequency transformer (a), as referred from the primary side (b)

eddy currents and hysteresis losses in the ferrite core are omitted [6, 7]. Capacitors C_1 and C_2 present self capacitances of the primary and secondary, respectively. Capacitor C_{12} depicts the transformer interwinding capacitance. The transformer has a turns ratio equal to n. To allow for an easier understanding of the oscillation phenomena, the equivalent-circuit parameters are transformed as referred from the primary side (Fig. 4b). The relations for parameter transformations are:

$$C_1' = C_1 + (1-n)\cdot C_{12} \tag{2}$$

$$C_{12}' = n \cdot C_{12} \tag{3}$$

$$C_2' = n^2 C_2 + n(n-1)C_{12} \tag{4}$$

$$L_{\sigma 2}' = \frac{1}{n^2}\cdot L_{\sigma 2} \tag{5}$$

As interwinding capacitance C_{12} is negligible and leakage inductance $L_{\sigma 2}'$ is small compared to main inductance L_m, the equivalent circuit is further simplified into

$$L_\sigma \approx L_{\sigma 1} + L_{\sigma 2}' \tag{6}$$

$$C_S \approx C_1' + C_2' \tag{7}$$

with overall stray capacitance C_S in parallel and only one leakage inductance L_σ in series on the transformer input. In this way we obtain a resonance circuit that causes primary-current oscillations. The resonant frequency depends on the leakage inductance and stray capacitance

$$f_{res} \approx \frac{1}{2\pi\sqrt{L_\sigma C_S}}. \tag{8}$$

These oscillations, when not suppressed, give rise to losses in the circuit and are the source of EMI. Combined with stray capacitance C_S and main inductance L_m, another system for mutual energy transfer is established. It becomes active in a certain time interval of the switching period [5].

4.3 Design Considerations of the Flyback Transformer

For the converter output voltage setting within its full range on the basis of the PWM control principle, the high-voltage high-frequency flyback transformer should be optimally designed. Designing such transformer by someone experienced only in usual step-down transformers with no knowledge of the discussed topic, is unfortunately a method of trials and errors. Our experimental work began with the flyback topology implementation. We quickly rearranged into a sub-optimal working forward topology. After inserting a new transformer into a satisfactorily working circuit, its performance worsened. This transformer was designed to meet the forward topology design considerations and consequently had a large number of turns and high turns ratio. This made us believe that the problems were due to the capacitive coupling between the primary and the secondary windings. Then we designed a new transformer with the U-shaped ferrite core thus making the windings spatial displacement possible. The solution was again a bad one as oscillations of a relatively low frequency were observed. After further researching we were able to design two similar transformers having the same parameters, except that one had an electrostatic screen placed between the primary and secondary windings. The one with no screen performed better. It enabled simpler setting of lower voltages.

When designing the last transformer our main target was to minimize the parasitic capacitances and leakage inductances. The most effective measure was already committed for other reasons but if carried out correctly it decreases the contribution of secondary self capacitance to the overall stray capacitance considerably. When the transformer secondary with the desired turns ratio of n is divided into four separate windings with the turns ratio $n/4$ each, the self capacitance of the separated winding is expected to be lower. When dependence is linear, however, it varies according to the turns configuration [8, 9], the capacitance of the separated secondary winding is a quarter of the capacitance of the unseparated winding

$$C_{2w1/4} = \frac{1}{4}C_2. \tag{9}$$

Also, if interwinding capacitance C_{12} is neglected, the self capacitance of all the four secondary windings as referred from the primary side is

$$C_{2w4/4}' = 4\cdot C_{2w1/4}' = 4\cdot\left(\frac{n}{4}\right)^2\cdot\frac{1}{4}C_2 = \frac{n^2}{16}\cdot C_2. \tag{10}$$

The U-shaped core was selected for having a wide window. The transformer was designed with no air-gap in order to obtain the desired inductance with the minimum number of primary turns. The converter supply voltage was high in order to minimize the turns ratio. We were thus able to construct each winding in only one layer with just small downsizing of the wire diameter determined compliably with the current

density recommendations. The secondary windings were all wound in the same direction to obtain the minimal capacitance between layers [8, 10]. The outer diameter of the experimental transformer with the electrostatic screen is bigger because of the additional layer of the used thin copper sheet and insulation. The leakage inductance is consequently higher. The main drawback of this transformer is the increase in the overall stray capacitance due to the presence of screen-winding capacitances.

5 EXPERIMENTAL RESULTS

The following experimental results allow for an insight into the principle of the switching converter operation and performance of the prototype source and provide some measurement results of the tested power semiconductor components.

5.1 Switching Converter Operation

Fig. 5 shows the photo of used flyback transformer constructed using the U-core of the following specifications: w = 44 mm, $h(1/2)$ = 37 mm, A = 150 mm^2, A_L = 3 µH. The number of turns of the primary and four secondary windings is 115, 193, 189, 185 and 178, respectively.

The oscillograms in Figs. 6, 7 and 8 show the waveforms of voltage U_{S4} of secondary S4, switching MOSFET drain-source voltage U_{DS}, gate-source voltage U_{GS} (Fig. 3) and primary current I_p for different operational states of the switching converter. Waveforms in Fig. 6 were taken at D = 50 % with the load on the source output terminals requiring 1.4 mA at 1320 V. The voltage on the converter output U_{HV} before protective resistor R_P, was 2120 V. The first part of primary current I_p charges the parasitic capacitor and the second part heaps the magnetic energy in the ferrite core of the flyback transformer.

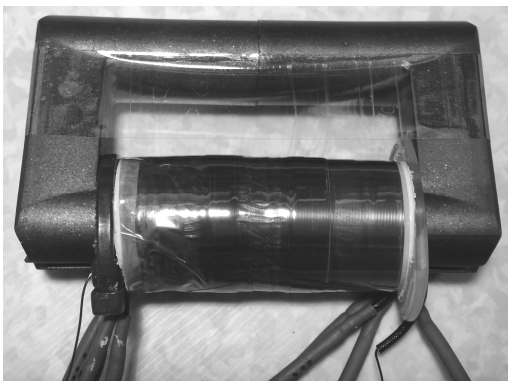

Figure 5. Photograph of used flyback transformer

Waveforms in Figs. 7 and 8 were taken at the same duty cycle D = 3.3 % and no load on the output terminals in order to demonstrate the difference between the normal turn-on of the switching MOSFET and turn-on at a decreased speed. Fig. 7 shows the waveforms at a decreased turn-on speed. We propose this solution in order to limit the charging current of the parasitic transformer capacitors and consequently to enable precise setting of the output voltage. "Low" frequency oscillations observed on the voltage waveforms are a consequence of energy exchange between the transformer parasitic capacitor and the main inductor. At the normal MOSFET turn-on (Fig. 8), high-frequency oscillations are observed. The frequency is some 5 MHz. The peak current is more than 1.5 A, whereas in the previous case it is less than 0.1 A. The output voltage is 420 V at a decreased turn-on speed, whereas at the normal turn-on, the output voltage is 1550 V.

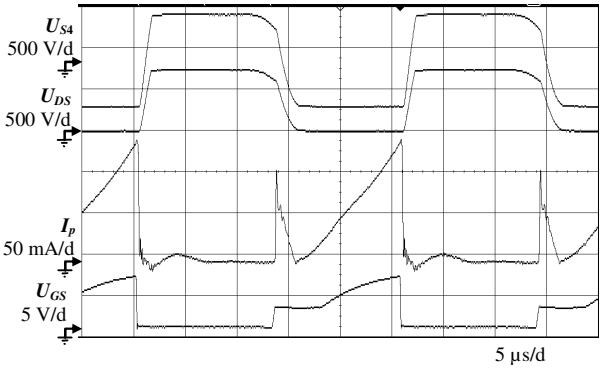

Figure 6. Waveforms of the loaded source, D = 50 %

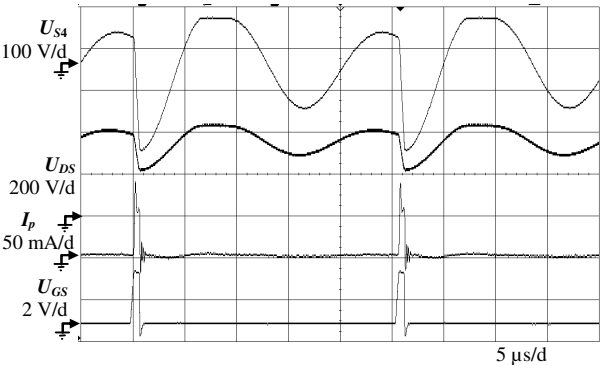

Figure 7. Waveforms of the unloaded source at a decreased MOSFET turn-on speed, D = 3.3 %

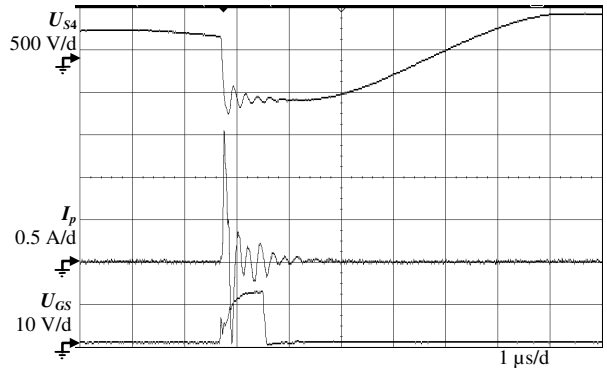

Figure 8. Waveforms of the unloaded source at a normal MOSFET turn-on speed, D = 3.3 %

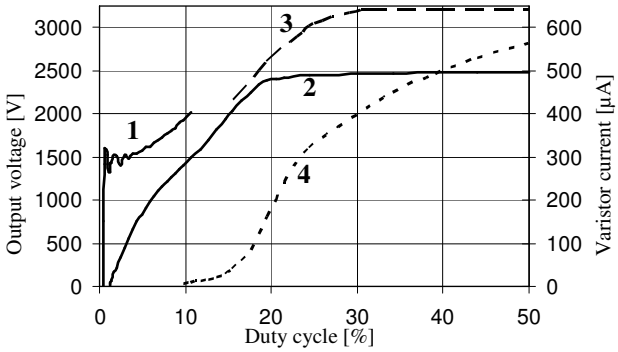

Figure 9. Graphs of the source output voltage: 1-normal MOSFET turn-on, 2/3-turn-on at a decreased speed with/without protecting varistors and 4-varistor current

Fig. 9. shows graphs of the output voltage of the unloaded source at normal turn-on and turn-on at a decreased speed of the switching MOSFET. The inability to set lower voltages at normal turn-on is clearly visible. Diagrams of the source output current and the switching converter output voltage are shown in Fig. 10. They were measured at the short-circuited output terminals. The converter maximum output power is 7 W.

5.2 Tests of Power Semiconductor Devices

Fig. 11 shows the reverse current of three types of 1000 V/1 A ultra fast switching diodes (UF4007, BYV26-E and MUR1100E) measured with our source. For current readings resolution above 2 µA, an external µAm has was used. Two specimens of each diode type were measured. The first two types performed in the usual way, while the MUR1100E diodes performed like high-ohmic resistors up to 1.3 kV. For the rectification in the switching converter we used MUR1100E diodes connected in series. Because of their special characteristic, there is no need to connect an additional voltage equalizing resistor in parallel with each diode.

In the second example, the HVDC source was used to test the SCR TYN608. Its nominal data are: $I_{T,av}$ = 5 A, $U_{DRM} = U_{RRM}$ = 600 V, $I_{DRM} = I_{RRM}$ = 5 µA at 25°C and I_{GT} within 2 mA and 15 mA. Measured I_D and I_R obtained at U_D and U_R = 1100 V were only 1.2 µA and at U_R = 1140 V I_R = 200 µA. The measured

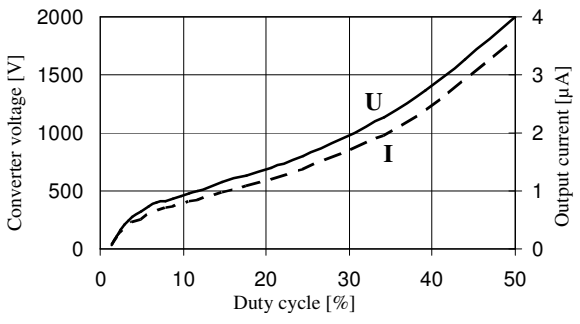

Figure 10. Source output current and the switching converter output voltage at short-circuited output terminals

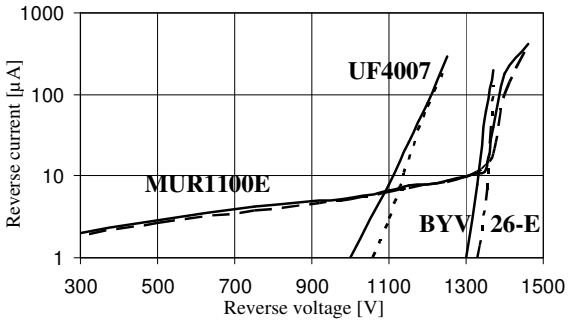

Figure 11. Reverse current versus the reverse voltage for similar ultra fast diodes

minimum gate current causing the preset direct voltage to collapse and the direct current to increase is shown in Table 1.

Table 1. Measured minimum gate trigger current versus the direct voltage for SCR TYN608

U_D [V]	300	600	1100
$I_{GT,min}$ [mA]	4.4	4.2	3.9

A photo of the laboratory prototype of the HVDC source is shown in Fig. 12. There are knobs for coarse and fine voltage setting on the left upper side. The on/off push button and knob for current limit setting are below. On the lower left side there are knobs for auxiliary current source setting and a switch for current/voltage-mode selection. On the right side below LCD there are output terminals and LEDs for supply and high voltage indication.

6 CONCLUSIONS

The described high-voltage DC source is a useful aid for laboratory needs and didactic purposes. It enables measuring reverse currents of diodes, SCRs and triacs, or direct currents in their blocking state. The used electrically insulated current source enables measuring the minimum triggering current dependence on the preset voltage of the main electrodes for SCR or triac in static conditions.

The switching power converter utilizes the flyback topology with a specially designed high-voltage transformer. Design considerations for the transformer with a minimum stray capacitance and leakage inductance are explained. Such transformer and the decrease in the speed of the switching MOSFET turning-on are essential factors for precise output-voltage control and reliable operation of the source.

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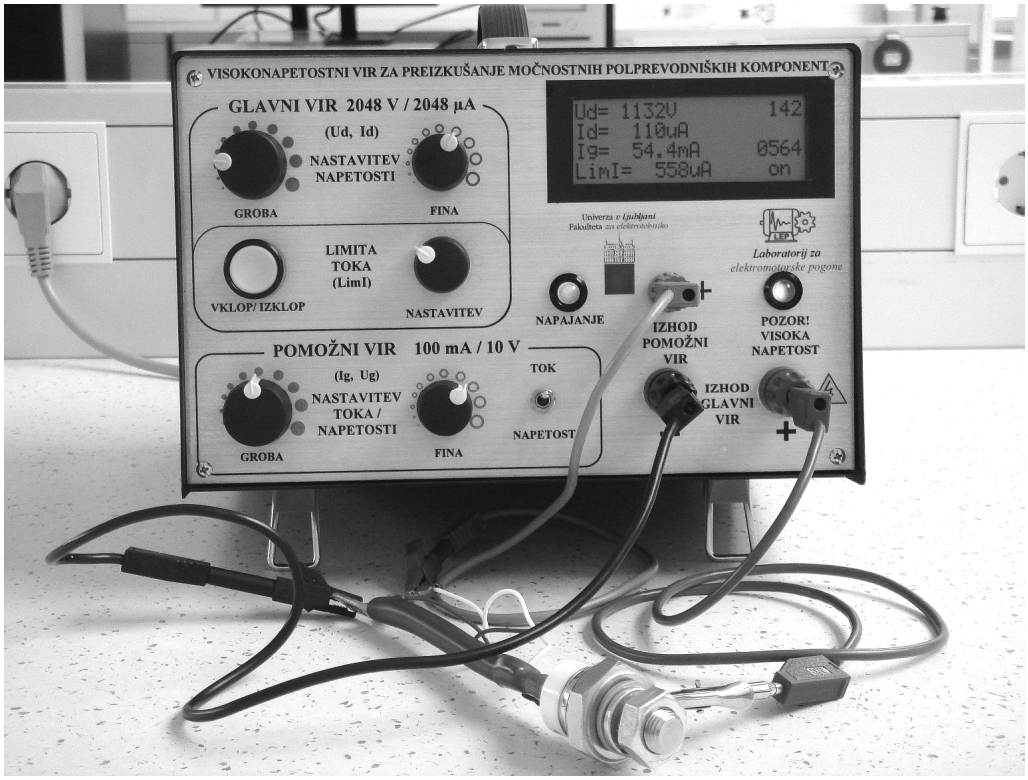

Figure 12. Laboratory prototype of the developed high-voltage DC source with SCR under test

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