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Mobility Modeling in a p-MOSFET under Uniaxial Stress

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Abstract. A semi analytical model describing the bulk mobility for holes in strained-p-Si layers as a function of applied uniaxial strain applied at the gate has been developed in this paper. The uniaxial tensile stress has been applied externally through the silicon nitride cap layer. The effects of uniaxial stress are understood on all the three components of mobility i.e. phonon, columbic and surface roughness mobility. The results show that the hole mobility is a strong rising function of applied uniaxial strain. Flatband voltage, Depletion Charge density, Inversion charge density, Energy gap and Effective surface electric field have been analytically modeled. There is a sharp increase in the vertical electric field and inversion charge density and decrease in the energy gap, depletion charge density and the flatband voltage when the uniaxial stress is applied. The hole mobility results have also been compared with the experimentally reported results and show good agreement. The results have also been compared with the electron mobility under the same conditions.

Keywords: mobility, strained-Si, model, experimental.

1 INTRODUCTION

CMOS technology has contributed significantly to the microelectronics industry thus playing an important role in the overall development of all the countries. The performance and density of a CMOS chip can be improved through device scaling which is inevitable as also propounded by Moore law which says that the transistor density on a CMOS chip doubles approximately after every one and a half years [1]. Continuing with the Moore law, the gate length of the MOSFET will eventually shrink to 10 nm in 2015 [2]. Seeing the trend of down scaling, continuous improvements in the VLSI MOSFET device models are required so that the exact behavior of deep sub-micron and nanometer scaled MOSFETs can be described with accuracy. The reduction in carrier mobility is a major cause of drain current degradation. But as we scale down the MOSFET, carrier mobility decreases due to the high vertical electric fields in the substrate. This reduces the speed of the device. To control these effects, strained silicon technology has evolved in the past few years as a replacement to silicon in substrate. on of extremely scaled down devices. The scaling down of both p-MOSFETs and n-MOSFETs has been taking place for their use in Complementary Metal Oxide Semiconductor (CMOS) technology. Very less attention has been given to the modeling process of p-MOSFET mainly because of the complex band structure of the valence band. Due to this reason, the hole inversion layers have not been studied and that too under uniaxial strain analytically. Various models/experiments have been developed in the past several years for the mobility estimation of the stressed silicon p-MOSFETs. Shifren et al [3] have experimentally and numerically shown the increase in the hole mobility on (100) oriented wafers. Uchida et al [4] have numerically evaluated the hole mobility in PMOS structures using k.p technique. Shuo et al [5] have experimentally found the hole mobility using uniaxial additive stress. Gaubert et al [6] have computed the hole mobility on (110) fabricated oriented wafers.

It would be appropriate to say here that there is a strong requirement of an analytical model which is simple and can be easily embedded into SPICE and largely accurate. An attempt has been made in this paper to semi analytically model the hole mobility under the condition of applied uniaxial strain at the gate.

2 STRAIN EFFECT ON MOBILITY

The deposition of a silicon nitride cap layer over the metal gate produces a uniaxial tensile strain. This is shown in Fig. 1.

The strain is a very useful parameter in devices as carrier mobility significantly increases due to the altering of the silicon band structure. The alteration of band structure in the channel layer provides lower

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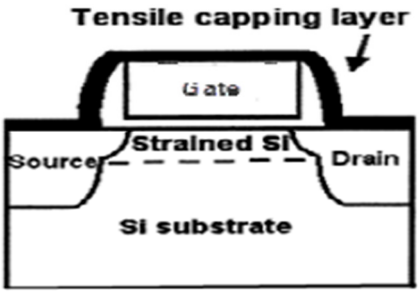

Figure 1.Cross-sectional view of uniaxial stressed-bulk-Si MOSFET.

effective mass and also suppresses intervalley scattering which is a prime cause of enhancement of carrier mobility and the drive current. Due to strain the valence bands split up into three sub bands. These are heavy hole, light hole and spin orbit hole sub bands as shown in Fig. 2.

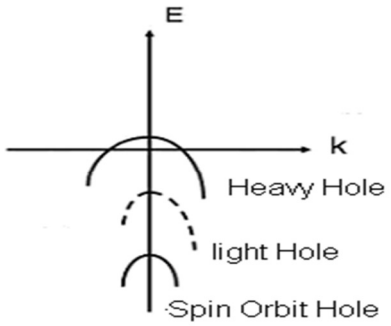

Figure 2. Energy band splitting due to uniaxial strain in silicon valence bands.

Due to strain, the effective mass of holes in the direction of flow of charge decreases and hence the mobility increases. Mathematically, carrier mobility is

$$\mu = q\,\tau/m^* \tag{1}$$

$1/\tau$ = scattering rate, m^* = Effective hole mass. The mobility is directly related to the carrier velocity v and applied external electric field E as shown by:

$$v = \mu E \tag{2}$$

It can be seen that increasing the carrier mobility increases the velocity, which is directly proportional to the switching speed of the device and the drain current. The bandgap of the silicon material falls as the uniaxial strain is applied as shown in Fig. 3.

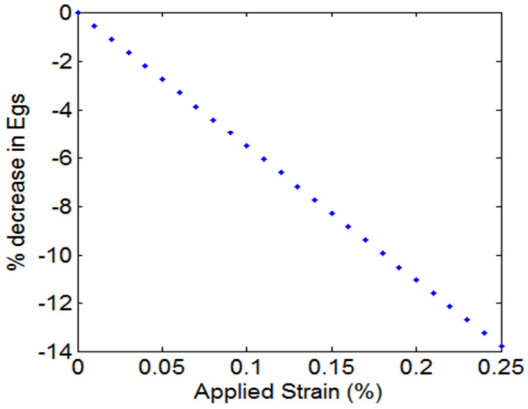

Figure 3. Percentage decrease in energy bandgap ((E_{gs}-E_g)/E_g)x100 with the applied strain (%) for uniaxial strained silicon MOSFETs at room temperature.

3 Modeling of Hole Mobility

Hole mobility is a very important parameter in the overall MOSFET modeling process. This is because parameters like drain current and hence trans-conductance strongly depend on mobility.

There are three major scattering mechanisms that affect a MOSFET's inversion layer carrier mobility given below.

3.1 Phonon scattering due to lattice vibrations

Phonon scattering is due to the lattice vibrations. The scattering rate is taken from [7]. The main problem is the calculation of the electric field at the oxide/silicon interface. Some of the parameters have been empirically modified to take the effect of uniaxial strain in the mobility calculations. The modified phonon scattering mobility is taken by modifying α to $\alpha(e)$ and β to β (e) by introducing the applied strain dependence:

$$\mu_{ph} = \mu_{PhB}\beta(e)\left[1+\left(\frac{E_{effs}}{E_0}\right)^{0.2\alpha(e)}\right]^{-1} \tag{3}$$

$$\mu_{phB} = 500\ cm^2/Vs$$

$$E_0 = 3\times 10^4\ V/cm$$

$$\alpha(e) = 1 + 1.28\times e - 0.16\times e^2$$

$$\beta(e) = 1 + 1.02\times e - 0.5\times e^2$$

E_{effs} is effective vertical electric field from the substrate to the oxide and "e" is the applied perpendicular tensile uniaxial strain.

3.2 Surface roughness scattering due to the microscopic roughness of the Si–SiO2 interface

The microscopic roughness at the surface of oxide/silicon interface causes a decrease in hole mobility due to scattering from the surface too. Moreover, the electric fields increasing due to the massive downscaling of the technology tend to pull the holes towards the interface further. The modified empirical formula for the surface roughness is obtained from [7] is given by modifying the δ parameter to δ(e) by introducing the strain dependence. The strain dependence has been done to accurately match the experimental results in the presence of uniaxial stress.

$$\mu_{sr} = \frac{\delta(e)10^{14}}{E_{effs}^2} \tag{4}$$

$$\delta(e) = \delta_0 + 3e - 1.2e^2$$

$$\delta_0 = 1.6$$

3.3 Coulomb scattering due to impurity scattering

The coulomb mobility from [5] as:

$$\mu_c = \left(C\frac{N_a}{N_s}\right)^{-1} \tag{5}$$

$$C = 70 \times 10^{-7}$$

$N_S = Q_{inv}/q$, $N_s$is electron density. N_a is doping concentration (cm^{-3})

The total mobility of the electrons is calculated as follows from the mathiessen's rule:

$$\mu_{Total}^{-1} = \mu_{ph}^{-1} + \mu_{sr}^{-1} + \mu_c^{-1} \tag{6}$$

4 Effective Surface Electric Field

First parameter in solving equations (3)-(5) is the surface electric field. The total charge density in the substrate (due to both inversion region and depletion region) is given by the Gauss law, and hence the surface electric field is found as:

$$E_{effs} = \left(\eta \times Q_{inv} + Q_{dep}\right)/\varepsilon_0\varepsilon_{si} \tag{7}$$

η = 1/3= correction in inversion charge density in (100) surface. Q_{inv} is the inversion charge density, Q_{depl} is the depletion charge density, ε_{si} is the relative permittivity of silicon substrate and ε_0 is the air permittivity. The below given Fig. 4 explains the dependence of the percentage rise in effective electric field with the applied strain at -3V gate voltage. The rise in vertical electric field is attributed to the fact that the more number of charge carriers will be available at a given electric field as compared to the conventional MOSFETs.

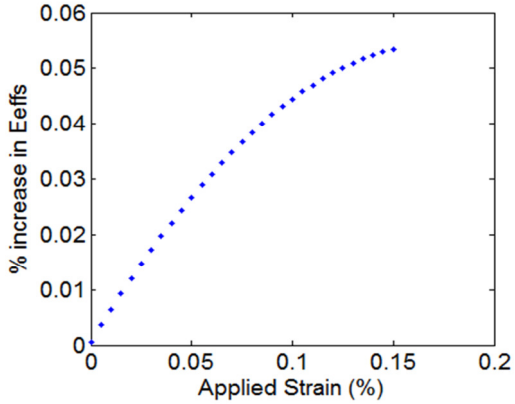

Figure 4. Percentage increase in surface electric field with applied strain at room temperature with a gate to source voltage of -3V.

4.1 Depletion Charge Density

The depletion charge density is given by solving Poisson Equation in the substrate in depletion region.

$$Q_{dep} = -\sqrt{2\varepsilon_0\varepsilon_{si}qN_a\phi_{ss}} \tag{8}$$

The below given Fig. 5 explains the dependence of the percentage fall in depletion charge density with applied uniaxial strain. This shows that the inversion layer will form at a lower gate voltage, thus reducing the overall threshold voltage of the MOSFET.

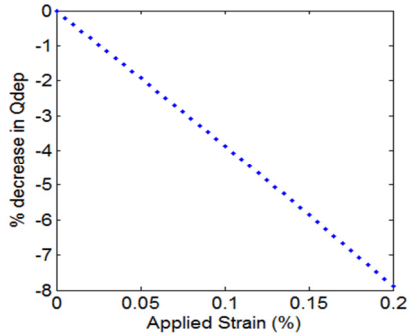

Figure 5 Percentage decrease in depletion charge with applied strain at room temperature for uniaxial strain silicon MOSFETs.

4.2 Inversion Charge Density

The inversion charge density is given by

$$Q_{inv} = C_{ox}(-V_{gs} + V_{ths}) \tag{9}$$

The below given Fig. 6 explains the dependence of the percentage rise in inversion charge density with applied uniaxial strain. This is due to the large decrease in the energy gap due to the applied strain, which forms the inversion layer fast.

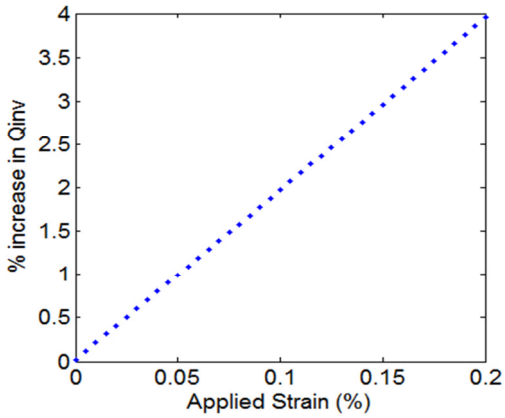

Figure 6. Percentage increase in inversion charge with applied strain at room temperature with a gate voltage of -3V.

$V_{ths}$is a uniaxial strained threshold voltage given by

$$V_{ths} = V_{fbs} - \phi_{ss} - \frac{Q_{dep}}{C_{ox}} \quad (10)$$

The flatband voltage V_{fbs} is given by

$$V_{fbs} = \left\{\phi_M - \left(X_s + \Delta E_g + \frac{E_g}{2q} - \phi_{fs}\right)\right\} - (Q_0/C_{ox}) \quad (11)$$

$X_s$is the electron affinity at the silicon substrate side and is increased due to decrease in energy gap, $\phi_{ss} = 2\phi_{fs}$,$E_g = 1.12$ eV, ΔE_g=-0.619e [8] .$\phi_{fs}$is given by $V_t ln(N_a/n_{is}), V_t = KT/q$, $n_{is} = n_i \exp(\Delta E_g/2KT)$, N_a=substrate concentration (cm^{-3}), $t_{ox}$is the oxide thickness (nm), Interface trap charge density, Q_0=8x10^{-5} C/cm^2. So, using (8)–(11) in (7), we get the effective surface electric field. So using (7),(3)–(6) can be solved explicitly.

The Fig. 7 explains the dependence of the percentage fall in flatband voltage with applied uniaxial strain. This is due to the large decrease in the energy gap due to the applied strain, which reduces the initial band bending between the gate material and the strained silicon substrate.

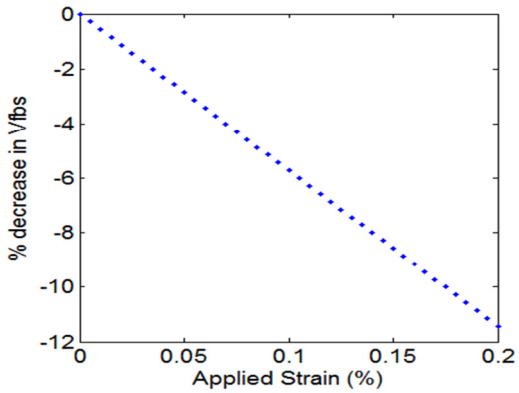

Figure 7. Percentage decrease in flatband voltage with applied strain at room temperature.

5 Results and Discussions

We have modeled hole mobility for the uniaxial strained silicon MOSFET for various device parameters. The parameters used in our simulation are given in Table 1. Figure 8 shows the phonon mobility variation with the effective surface electric field. The influence of strain due to increased applied uniaxial strain is clearly seen as the mobility increases with the increased perpendicular tensile strain even at high electric fields. So the applied strain reduces the phonon scattering mechanism in the inversion layer of MOSFETs. The arrow in Fig. 8 shows the large increase in the phonon mobility as the percentage of applied strain is large.

Table 1.Strained Silicon MOSFET parameters used in simulation.

Parameter	Value
Apllied Strain	0–0.25%
Source/Drain and poly silicon doping	$2\times10^{20}cm^{-3}$
Substrate doping	$10^{17}cm^{-3}$
Gate oxide thickness	8.0nm
Workfunction of gate material	4.2 eV

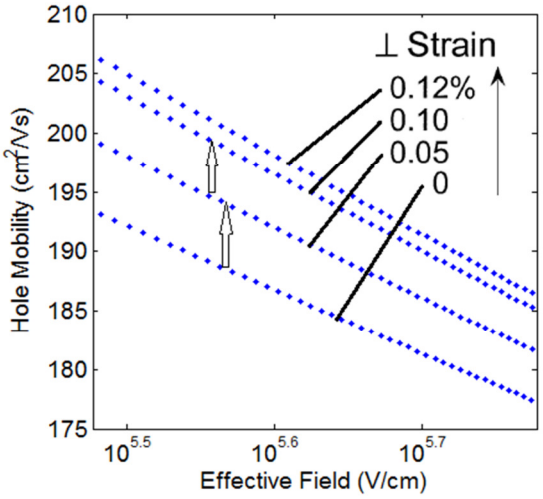

Figure 8. Modeled results of hole phonon mobility with effective electric field for the p-MOSFETs under transverse (perpendicular) uniaxial tensile strain at room temperature.

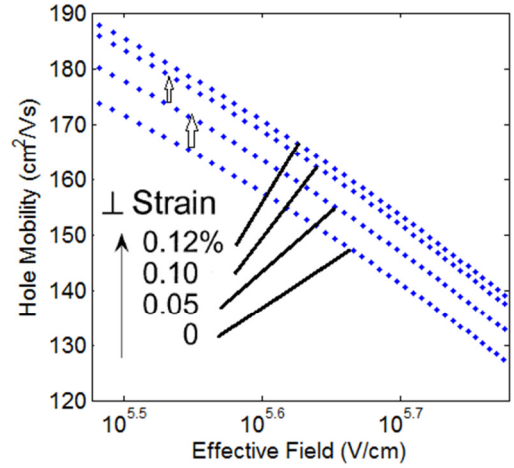

Figure 9. Modeled results of hole mobility (accounting for phonon and surface roughness scattering mechanisms) with effective electric field for the p-MOSFETs under (perpendicular) strain at room temperature.

Figure 9 shows the hole mobility (accounting for phonon and surface roughness scattering mechanism) with effective surface electric field at room temperature. The influence of strain is clearly seen as the hole mobility including phonon and surface roughness scattering mechanism increases with the increased percentage of applied transverse strain even at high electric field. So the surface roughness scattering mechanism is also reduced with the applied strain. The arrow in Fig. 9 shows the large increase in the mobility as the percentage of applied strain is large. Figure 10 shows all the three mobility variation with the effective surface electric field. The influence of strain is clearly seen as the surface hole mobility increases with the increased percentage of strain even at high electric fields. The results match closely with reported results [9].

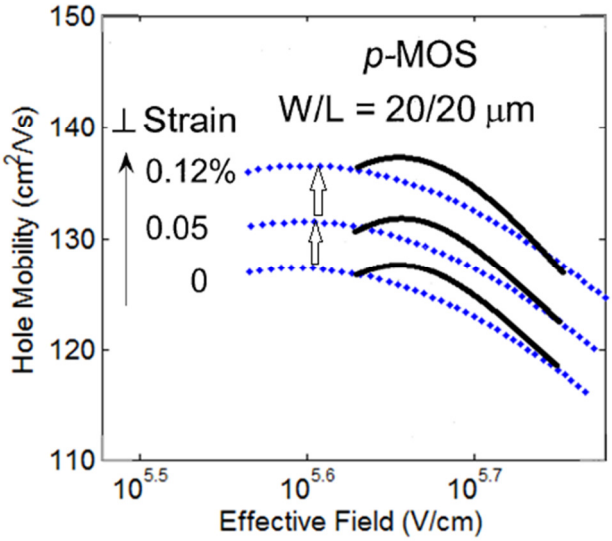

Figure 10 Modeled results of hole mobility with effective electric field for the p-MOSFETs under transverse (perpendicular) strain at room temperature. Experimental results reported in [9] are shown by black lines. Our results are shown by doted blue lines. The results show good agreement with the reported results.

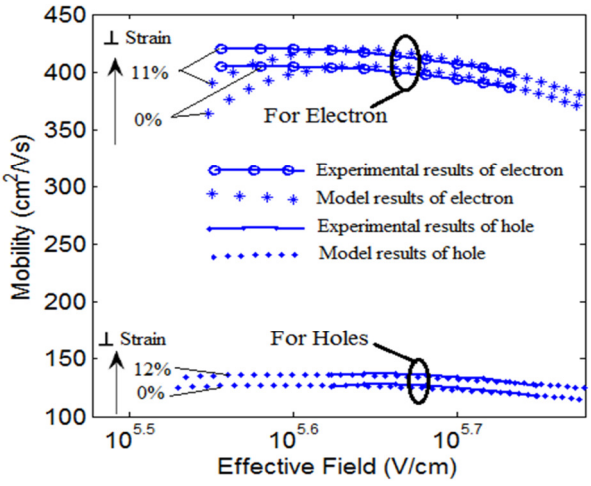

Fig 11 Modeled results of hole mobility with effective electric field for the p-MOSFETs under transverse (perpendicular) strain at room temperature. Experimental results reported in [9] are shown by black lines. Our results are shown by doted blue lines. The results show good agreement with the reported results.

Figure 11 shows all the three mobility variation with the effective surface electric field. The influence of strain is clearly seen as the surface hole mobility increases with the increased percentage of strain even at high electric fields. The corresponding results for the electrons show a higher mobility under similar conditions. The results match closely with reported results [9] for both electrons [10] and holes.

6 CONCLUSION

All the major electric parameters such as flatband voltage, inversion and depletion charge density etc, have been modeled .The semi analytical model developed in this paper shows an increase of hole mobility with the applied uniaxial strain at a given electric field. The results match closely with the experimental reported results thus proving the validity of the model.

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