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Effective Controller Design for the Cascaded H-bridge Multilevel DSTATCOM for Reactive Compensation in Distribution Utilities

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Abstract. The Static Synchronous Compensators (STATCOMs) have been recoginzed as the most effective solution for dynamic reactive power compensation, voltage stability enhancement and subsynchronous resonance damping purposes in the electric power systems. The STATCOMs in the distribution utilites (DSTATCOMs) are increasingly investigated for dynamic reactive power compensation and power quality improvement in the distribution utilites. This paper presents a novel control scheme for the cascaded H-bridge (CHB) DSTATCOM. The principle of the carrier phase-shifted pulse-width modulation (CPS-PWM) and the mathematical model of the CHB-DSTATCOM are presented. The power balancing mechanism and the stable control region are analyzed. The current loop controller and the dc-link voltage balancing controller are synthesized and the design guidelines are provided. The simulation results obtained from the Electromagnetic Transient Program / Alternative Transient Program (EMTP/ATP) are presented and evaluated, which verifies the validity and effectiveness of the devised control scheme.

Keywords: Multilevel inverter, cascaded H-bridge, reactive power compensation, PLL, DSTATCOM, adaptive filter, EMTP/ATP

1 INTRODUCTION

In recent years, the power quality issues have become important topic due to the proliferation of disturbing loads, which causes significant voltage fluctuations, sag/swell and temporary interruptions. To mitigate the voltage disturbance problems, the static synchronous compensator (STATCOM) are the most suitable solutions, which can be installed at the transmission networks or at the distribution networks to protect the voltage sensitive loads.

Due to its modularity and flexibility of manufacturing, the cascaded H-bridge (CHB) inverter is appreciated for high-power medium-voltage power quality conditioner applications. However, restricted by the limited switching frequency of the power electronic devices, achieving dc-link voltage balancing and sufficient controller bandwidth is rather complicated [1-3, 5].

The design guidelines for CHB-DSTATCOM have not been reported in the previous literatures. Hence, this paper aims to cover this gap. The analysis for active and reactive power distribution between the two cells is presented. Based on the power balancing mechanism, a novel dc-link voltage control scheme is proposed by splitting the control task into two parts, i.e., the average voltage controller and voltage balancing controller. A novel grid-synchronization scheme based on the adaptive linear neural network (ADALINE) is devised to acquire the phase angle of grid voltage [4]. Simulation results obtained from the alternative transient program (ATP) are provided, which verifies the validity and effectiveness of the devised control scheme.

2 PRINCIPLE OF THE CARRIER PHASE-SHIFTED PWM

Fig.1 shows the circuit diagram of the five-level cascaded multilevel DSTATCOM based on two H-bridge modules. In Fig. 1, L_g and R_g indicate the line impedance. Each H-bridge includes four IGBT switches with anti-parallel diodes and a dc-link capacitor. Thus the output voltages of the CHB-DSTATCOM can be derived as: $v_{aN}=v_{a1}+v_{a2}$.

Assuming $v_{dc1}=v_{dc2}=V_{dc}$ in steady state and the unipolar modulation scheme is adopted in the PWM process, thus each H-bridge would produce three voltage levels: $-V_{dc}$, 0, V_{dc}. With reference to the upper bridge, it is possible to set $v_{a1}=+V_{dc}$ by turning on

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switches S_{11} and S_{14} and v_{a1}=-V_{dc} by turning on switches S_{12} and S_{13}. Moreover, it is possible to set v_{a1}=0 by turning on either S_{11} and S_{12} or S_{13} and S_{14}, the lower bridge operates in a similar manner. Thus five distinct voltage levels can be synthesized at the ac terminals. It is worth noticing that, the switching states of S_{x1}, S_{x2} (x=1, 2, 3) must be complementary to those of S_{x3}, S_{x4} (x=1, 2, 3) in order to avoid short circuit of the H-bridges [2, 3].

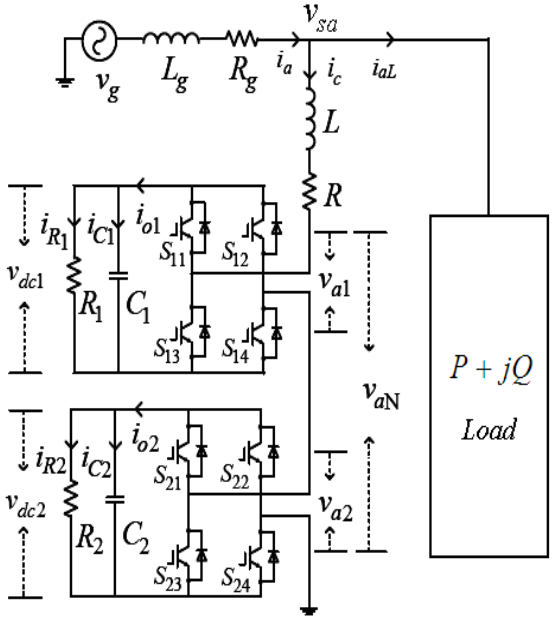


Figure 1. Block diagram of the cascaded H-bridge multilevel DSTATCOM.

To obtain five level output voltage at the ac terminal, the carrier signals utilized in each cell must be phase shifted by 90 degree in case of two H-bridge module configuration. Fig.2(a) shows the waveforms of the modulation signal, phase-shifted carriers and the output multilevel voltage of the CHB-DSTATCOM. Fig.2(b) shows the enlarged view of Fig.2(a) including the gating signals of the first IGBT for each H-bridge inverter.

Notably, the variables in this paper are as follows:
t:CTR_H1→The modulation signal of the first cell;
t:CTR_H2→ The modulation signal of the second cell;
t:VTRI→The carrier signal of the first cell;
t:VTR_2→ The carrier signal of the second cell;
v: 'VOUT -'→The synthesizes multilevel voltage 'v_{aN}';
t: 'SIG1'→The gating signal for IGBT S11;
t: 'SIG5'→The gating signal for IGBT S21;
t:VBC_H1→The output of the first VBC controller;
t:VBC_H2→The output of the second VBC controller;
t:P1, t:P2→The output of the average voltage controller;
t:VDC1→The dc-link voltage in the first inverter;
t:VDC2→The dc-link voltage in the second inverter;
c: 'SA -MA'→The grid side current;
t: IS_REF →The reference signal for the grid current;
t: IS_ERR →The grid side tracking error;
It should be noticed that, the scaling factors and offsets of these signals are marked at the bottom of each figure.

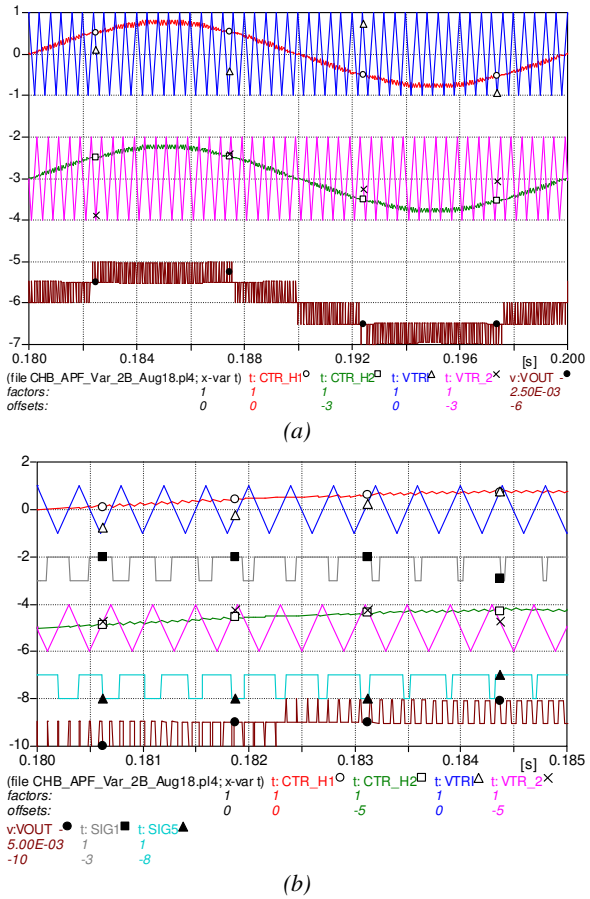


Figure 2. The simulated waveforms of the CHB-DSTATCOM: (a) The waveform of the modulation signal, phase-shifted carriers and the output multilevel voltage; (b) The enlarged view of (a) including the gating signals of the first IGBT for each H-bridge inverter.

3 THE MODEL DERIVATION OF CHB-DSTATCOM

Referring to Fig.1, the switching functions of the multilevel CHB-DSTATCOM can be derived as [2, 3]:

$$\begin{cases} f_1 = S_{11} \cdot S_{14} - S_{12} \cdot S_{13} \\ f_2 = S_{21} \cdot S_{24} - S_{22} \cdot S_{23} \end{cases} \quad (1)$$

The value of f_x (x=1, 2) indicates the dynamic process of charging and discharging between the dc-link capacitors C_1 and C_2. Supposing the DSTATCOM current i_c is positive, then the capacitor C_x (x=1, 2) is charging if f_x=1, discharging if f_x =-1, and not undergoing any of these processes if f_x=0. Complementary phenomenon appears if the inverter current is negative. The following assumptions are made for deriving the model of the cascaded H-bridge inverters:

(a)The grid is assumed to be AC voltage source;

(b)The losses of the multilevel DSTATCOM are categorized as effective series loss and parallel loss. The series loss and interfacing inductor loss are represented as equivalent series resistance (ESR). Parallel losses are represented as shunt connected resistances across the

dc-link capacitors, corresponding to the active power loss of the H-bridge, including blocking loss, capacitor loss and absorbing circuit loss, etc.

The differential equation describing the dynamics of the coupling inductor between the cascaded H-bridge inverter and the grid is derived as [5]:

$$v_{sa} = Ri_c + L\frac{di_c}{dt} + f_1 v_{dc1} + f_2 v_{dc2} \tag{2}$$

where the variable v_{sa} represents grid voltage at the point of common coupling (PCC) [see Figure 1], L represents the inductance of the coupling inductor and R represents the equivalent series resistance. The variables v_{dc1} and v_{dc2} are the actual voltages across the dc-link capacitors of the cascaded H-bridge inverter, which may not equal to the reference voltage during dynamic process. According to the Kirchoff's law, the currents flowing into the dc-link capacitors C_1 and C_2 can be expressed as:

$$\begin{cases} i_{C1} = C_1\dfrac{dv_{dc1}}{dt} = i_{o1} - i_{R1} = f_1 i_c - \dfrac{v_{dc1}}{R_1} \\ i_{C2} = C_2\dfrac{dv_{dc2}}{dt} = i_{o2} - i_{R2} = f_2 i_c - \dfrac{v_{dc2}}{R_2} \end{cases} \tag{3}$$

where R_1 and R_2 are the equivalent resistance of each H-bridges, representing the parallel losses. The variables i_{o1} and i_{o2} represent the total dc-link current and i_{R1} and i_{R2} represent the currents in the dc-link resistance of the individual H-bridge module. Let the vector of state variables as $X_2=[i_c,\ v_{dc1},\ v_{dc2}]^T$ and $U_2=[v_{sa},\ 0,\ 0]^T$, as input vector, rearranging Eqs.(1)-(3), the state equations can be rewritten in the compact matrix form as:

$$\dot{X}_2 = \mathbf{A}_2 X_2 + \mathbf{B}_2 U_2 \tag{4}$$

where

$$\mathbf{A}_2 = \begin{bmatrix} -\dfrac{R}{L} & -\dfrac{f_1}{L} & -\dfrac{f_2}{L} \\ \dfrac{f_1}{C_1} & -\dfrac{1}{R_1 C_1} & 0 \\ \dfrac{f_2}{C_2} & 0 & -\dfrac{1}{R_2 C_2} \end{bmatrix},$$

$$\mathbf{B}_2 = \begin{bmatrix} \dfrac{1}{L} & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix}.$$

4 THE ANALYSIS OF POWER BALANCING MECHANISM

Fig.3 shows the equivalent circuit of the multilevel CHB-DSTATCOM for the steady-state power balance analysis. In Fig.3, the individual H-bridge inverters are represented by AC voltage sources v_{a1} and v_{a2}, which are derived as [2, 3]:

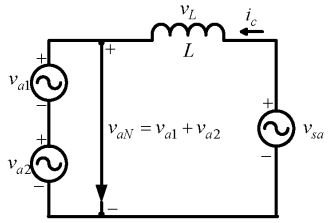


Figure 3. The equivalent circuit diagram of the CHB-DSTATCOM.

$$\begin{cases} v_{a1} = f_1 v_{dc1},\ p_{R1} = v_{dc1} i_{R1} \\ v_{a2} = f_2 v_{dc2},\ p_{R2} = v_{dc2} i_{R2} \end{cases} \tag{5}$$

where p_{R1} and p_{R2} represents the active power consumed by the effective resistance across the dc-link capacitors. For the sake of brevity, the equivalent resitance of the coupling inductor is neglected, hence Eq.(2) can be rewritten as:

$$v_{sa} = L\frac{di_c}{dt} + v_{a1} + v_{a2} \tag{6}$$

From Fig.1 and Fig.3, the power balancing equations of the CHB-DSTATCOM can be derived as:

$$v_{a1} i_c = C_1 \frac{d}{dt}\left(\frac{v_{dc1}^2}{2}\right) + p_{R1} \tag{7}$$

$$v_{a2} i_c = C_2 \frac{d}{dt}\left(\frac{v_{dc2}^2}{2}\right) + p_{R2} \tag{8}$$

The behavior of the CHB-DSTATCOM is charaterized by the inductor current dynamics and the dc-link capacitor voltage dynamics. The power balance between the two H-bridge inverters depends on the dc-link voltages and the individual modulation signals. To better illustrate the mechanism of power exchange between the two modules, the phasor diagram of the output voltages and current of the CHB-DSTATCOM is given in Fig.4. In the analysis, it is assumed that v_{aN} is calculated in such a way that i_c is 90 degree phase-shifted with respect to v_{sa}. The angles θ_1 and θ_2 represent the phase shifts of the output voltages v_{a1} and v_{a2} with respect to v_{sa}, leading to a reactive power exchange between the individual H-bridge inverter with the grid.

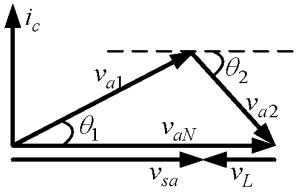


Figure 4. The phasor diagram of the voltages and current.

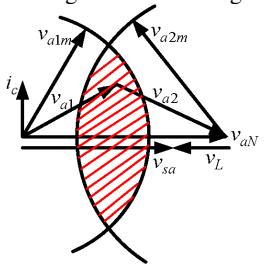


Figure 5. The stable control area of the CHB-DSTATCOM.

In the phasorial diagram (Fig.4), the maximum output voltages in root-mean square (rms) values of each H-bridge can be calculated as:

$$v_{a1m} = \frac{4}{\pi\sqrt{2}} v_{dc1},\ v_{a2m} = \frac{4}{\pi\sqrt{2}} v_{dc2} \quad (9)$$

The reactive power injected by each H-bridge inverter to the grid depends on the value of the capacitor voltage in the cell and the control signal modulated by each module. To ensure stable operation of the CHB-DSTATCOM, both cells must be utilized to synthesize the output voltage v_{aN}.

Fig.5 shows the red marked area the possible points to achieve the desired output voltage. Any point outside of this region makes the system unstable since the output voltage of the CHB-DSTATCOM cannot be modulated with those values of the dc-link capacitor voltages. Furthermore, as shown in Fig.5, the projections of v_{a1} and v_{a2} over v_{sa} are always positive. Hence, the reactive powers in both converters are positive, indicating that both inverters of CHB-DSTATCOM inject reactive power to the grid simultaneously. Moreover, it is not possible to find a point where one of the cells injects reactive power and, at the same time, the other cell absorbs reactive power from the grid.

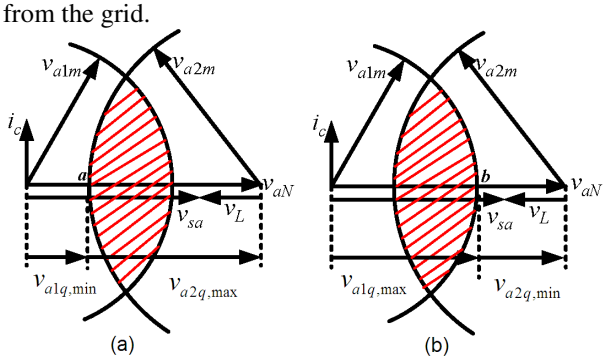


Figure 6. The diagram of maximum and minimum reactive power limits.

Fig.6 shows that, for a given total amount of reactive power to be supplied or absorbed by the H-bridge inverter, the reactive power sharing by each cell has to be between a minimum and maximum value to achieve a stable operation of the CHB-inverter. Fig.6(a) shows the minimum reactive power supplied by the first inverter, which corresponds to the minimum reachable length of the projection of v_{a1} over v_{sa}, represented by $v_{a1q,min}$. As the amount of reactive power supplied by the CHB-DSTATCOM is fixed, this value is related with the maximum reactive power that is supplied to the second cell, shown in Fig6(a) as $v_{a2q,max}$, which is the maximum reachable length of the projection of v_{a2} over v_{sa}. In the same way, the values for the maximum reactive power supplied by the first inverter $v_{a1q,max}$ and the minimum reactive power supplied by the second inverter $v_{a2q,min}$ can also be illustrated, as shown in Fig.6(b).

5 CONTROLLER SYNTHESIS METHODOLOGIES

Based on the analysis of the power balancing mechanism, the control block diagram can be synthesized, as shown in Fig.7. The control algorithm consists of five blocks, i.e., the reference current generation (RCG) unit, the phase-locked loop (PLL), the current loop controller (CC), the average dc-link voltage controller (AVC) and the dc voltage balancing controller (VBC). Further, the voltage balancing scheme based on the AVC and VBC control achieves equal reactive power sharing of the two cells by dynamically exchanging active power within the two inverters, and the outputs of the AVC controller (P_1 and P_2) are applied to the VBC controller to regulate the difference of dc voltages.

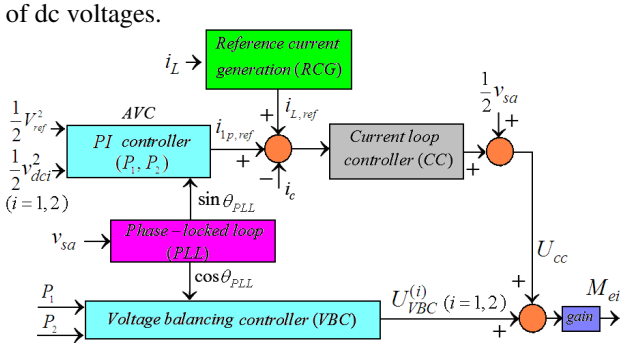


Figure 7. The block diagram of the devised control algorithms.

5.1 Novel Phase-locked Loop (PLL) based on Adaptive Linear Neural Network (ADALINE)

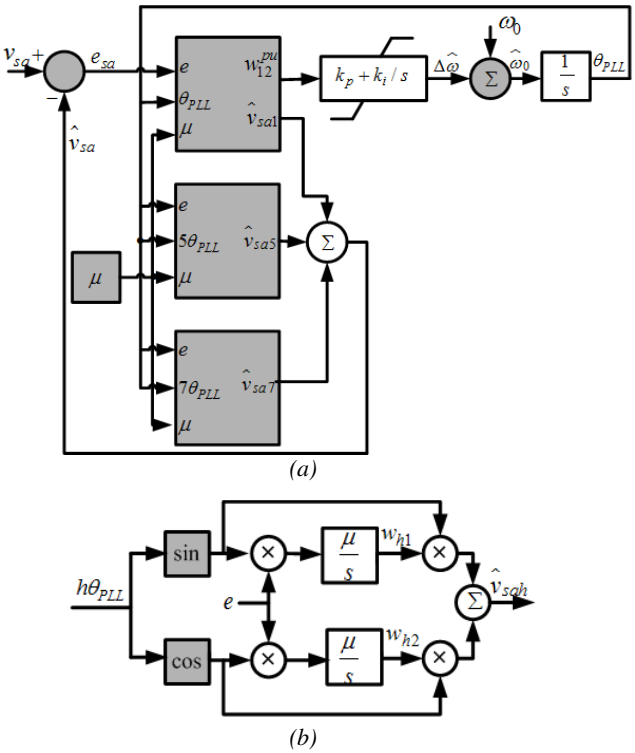


Figure 8. The proposed ADALINE-PLL (APLL) (a) overview of the APLL;(b)the block diagram for the *h*th order harmonic component

Accurate synchronization of the multilevel CHB-DSTATCOM to the grid is vital to ensure its stable operation since the phase angle of the grid voltage was utilized to achieve the active and reactive power balancing for the individual H-bridge modules. Fig.8 shows the diagram of the ADALINE-based PLL for grid synchronization based on the least-mean square (LMS) estimation algorithm [4]. Here the mathematical formulation of the APLL is briefly outlined. An arbitrary grid voltage can be represented as:

$$v_{sa}(t) = V_1 \sin(\omega_0 t + \varphi_1) + \sum_{n=2}^{N} V_n \sin(n\omega_0 t + \varphi_n) \quad (10)$$

where φ_1 and φ_n are the initial phase angle of the fundamental and nth order harmonic component, respectively. The dc offset is neglected for the sake of brevity. The phase angle of the fundamental component voltage can be expressed as $\varphi_1=\Delta\theta_1+\theta_1$, where θ_1 and $\Delta\theta_1$ represent the estimated phase angle of the fundamental grid voltage and the estimation error, respectively, obtained from the APLL. Therefore, the phase angle of the nth order harmonic component can be expressed as:

$$\begin{aligned} n\omega_0 t + \varphi_n &= n(\omega_0 t + \theta_1) + \varphi_n - n\theta_1 \\ &= n(\omega_0 t + \theta_1) + n\Delta\theta_1 + (\varphi_n - n\varphi_1) \end{aligned} \quad (11)$$

where φ_n is the initial phase angle of the nth order harmonic component. Substituting Eq.(11) back into (10), rearranging terms, we get [4]:

$$\begin{aligned} v_{sa}(t) &= V_1 \cos(\Delta\theta_1)\sin(\omega_0 t + \theta_1) \\ &+ V_1 \sin(\Delta\theta_1)\cos(\omega_0 t + \theta_1) \\ &+ \sum_{n=2}^{N} \{V_n \cos(n\Delta\theta_1 + (\varphi_n - n\varphi_1))\sin[n(\omega_0 t + \theta_1)]\} \\ &+ \sum_{n=2}^{N} \{V_n \sin(n\Delta\theta_1 + (\varphi_n - n\varphi_1))\cos[n(\omega_0 t + \theta_1)]\} \end{aligned} \quad (12)$$

From (12), it can be deduced that the original signal denoted by Eq.(10) can be regenerated by adjusting the coefficients $V_n\cos(n\Delta\theta_1+(\varphi_n-n\varphi_1))$, $V_n\sin(n\Delta\theta_1+(\varphi_n-n\varphi_1))$ (n=1, …, N), even though the phase angle of the original signal is unknown.

The weight vector W denotes the coefficients of the corresponding trigonometric functions. From the above defintion, the fundamental grid voltage can be expressed as: $\hat{Y} = W^T X$, where $\hat{Y}$ is the estimated output of the fundamental grid voltage by using the LMS-based weights estimation scheme. The vector W and X corresponding to the weight vector and the input vector, respectively, are represented as:

$$\begin{cases} W = [V_1\cos(\Delta\theta_1), V_1\sin(\Delta\theta_1), \ldots, \\ \quad V_n\cos(n\Delta\theta_1 + (\varphi_n - n\varphi_1)), \\ \quad V_n\sin(n\Delta\theta_1 + (\varphi_n - n\varphi_1))] \\ \quad = [\omega_{11}, \omega_{12}, \ldots, \omega_{n1}, \omega_{n2}] \\ X = [\sin(\omega_0 t + \theta_1), \cos(\omega_0 t + \theta_1), \ldots, \\ \quad \sin[n(\omega_0 t + \theta_1)], \cos[n(\omega_0 t + \theta_1)]]^T \end{cases} \quad (13)$$

From Eq.(13), the weights of the fundamental frequency component are denoted as ω_{11} and ω_{12}, hence the phase estimation error denoted by $\Delta\theta_1$ can be regulated to zero by using a properly designed closed-loop control system, which resembles that of the existing grid synchronization schemes. As shown in Fig.8(a), the per unit representation of the weight ω_{12} is utilized as the input signal for the loop filter (LF) of the APLL, derived as [4]:

$$\begin{aligned} \omega_{12}^{pu} &= \frac{\omega_{12}}{\sqrt{\omega_{11}^2 + \omega_{12}^2}} \\ &= \frac{V_1 \sin(\Delta\theta_1)}{\sqrt{V_1^2 \sin^2(\Delta\theta_1) + V_1^2 \cos^2(\Delta\theta_1)}} = \sin(\Delta\theta_1) \end{aligned} \quad (14)$$

The weights updating process of the proposed APLL is similar to the adaptive linear neural network (ADALINE), which was based on the recursively searching the optimal point of the quadratic cost function, i.e., the least square (LS) error. Notably, the difference between the ADALINE algorithm and the proposed APLL is that, the frequency and phase angle signals utilized in the ADALINE weights updating process were assumed to be constant. However, in case of the APLL, the frequency and phase angle of the fundamental grid voltage is recursively updated by the loop filter (LF) and voltage controlled oscillator (VCO) [Fig.8].

5.2 Current Loop Controller Design

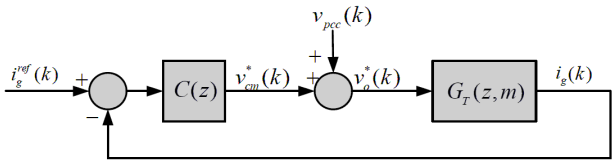


Figure 9. The closed-loop block diagram of the current tracking loop.

Fig.9 shows the discrete control diagram of the current loop controller for the CHB-DSTATCOM, where the transfer function C(z) represents proportional-integral (PI) regulator:

$$C(z) = k_p + \frac{k_i T_s}{z-1} \quad (15)$$

where k_p and k_i denote the proportional and integral gains. The plant of the current controller is the coupling inductor, and $G_p(s)=1/(L_0 s+R_0)$, where L_0 and R_0 denote the nominal parameters. Eq.(6) can be discretized using the zero-order hold (ZOH) method, as:

$$\begin{aligned} G_T(z,m) &= Z\left\{\underbrace{\frac{1-e^{-sT_s}}{s}}_{H(s)} G_p(s) e^{-smT_s}\right\} = \frac{z-1}{z} Z\left\{\frac{G_p(s)}{s} e^{-smT_s}\right\} \\ &= \frac{z-1}{z} Z_m\left\{\frac{G_p(s)}{s}\right\} = \frac{T_s/L_0 \cdot z^{-m}}{z-(1-R_0 T_s/L_0)} \end{aligned} \quad (16)$$

where 'm' denotes the equivalent sample of control delay. Neglecting the effect of the grid voltage and

consider m=1, the open loop transfer function of the current loop controller can be derived as:

$$G_{open}^{cc}(z)=\frac{k_pT_s}{L_0}\cdot\frac{z-(1-(k_iT_s/k_p))}{z(z-1)[z-(1-(R_0T_s/L_0))]} \quad (17)$$

Hence, the closed-loop transfer function can be easily derived from Eq.(17).

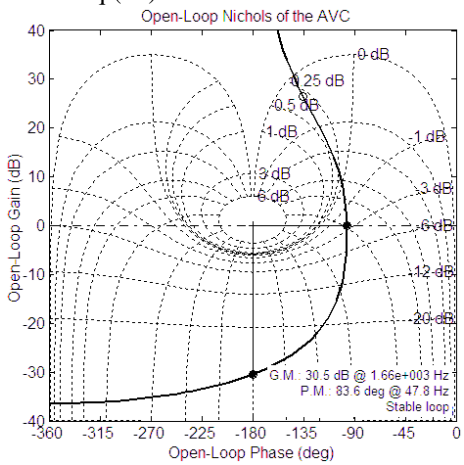


Figure 10. The open-loop Nichols diagram of the average voltage controller (AVC) when T_c=100μs.

5.3 Voltage balancing controller design

The voltage regulation loop includes the average voltage controller (AVC), which is designed to regulate the total active power balance between the CHB-DSTATCOM with the grid, and the voltage balancing controller (VBC), which is designed to regulate active power exchange between the two H-bridge inverters and achieve the equal reactive power sharing for the two cells.

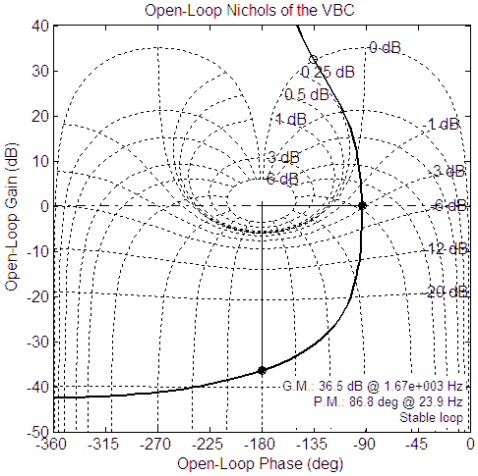
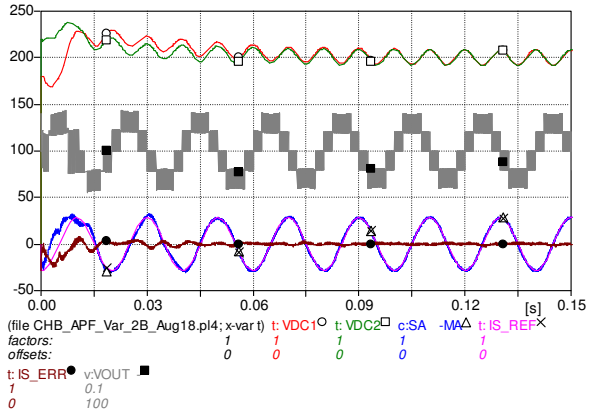


Figure 11. The open-loop Nichols diagram of the voltage balancing controller (VBC) when T_c=100μs.

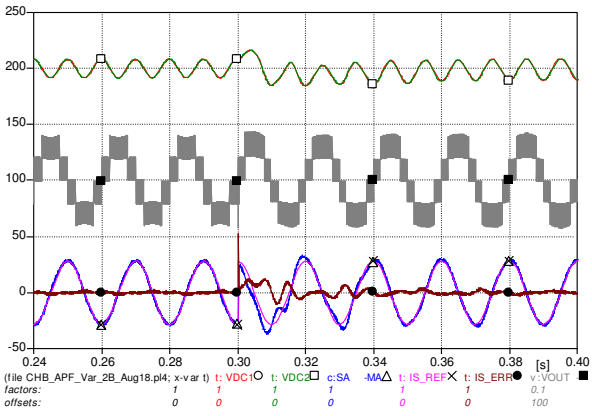
Fig.10 shows the open-loop Nichols diagram of the AVC, where the proportional -integral parameters are designed as $k_{p,AVC}$=0.6, $k_{i,AVC}$=12. It shows that a gain margin (GM) of 30.5dB and a phase margin (PM) of 83.6 degree is achieved. Hence the AVC loop is stable. Fig.11 shows the open-loop Nichols diagram of the VBC, where the proportional- integral parameters are designed as $k_{p,VBC}$=0.1, $k_{i,VBC}$=1.2. It shows that a gain margin (GM) of 36.5dB and a phase margin (PM) of 86.8 degree is achieved, thus the stability of the VBC loop is guaranteed.

6 SIMULATION RESULTS AND DISCUSSIONS

In order to verify the effectiveness of the devised control scheme, digital simulation using the Alternative Transient Program (ATP/EMTP) was performed and the results are evaluated. The parameters of the system are: L_g=50μH, R_g=20mΩ, L=1.5mH, R=50mΩ, and the nominal dc-link parameters are: C_1=C_2=2000μF, R_1=R_2=39000Ω, sampling time T_s=100μs, the grid voltage v_{sa}=220V(rms), the target inverter dc-link voltage is 200V.



(a)

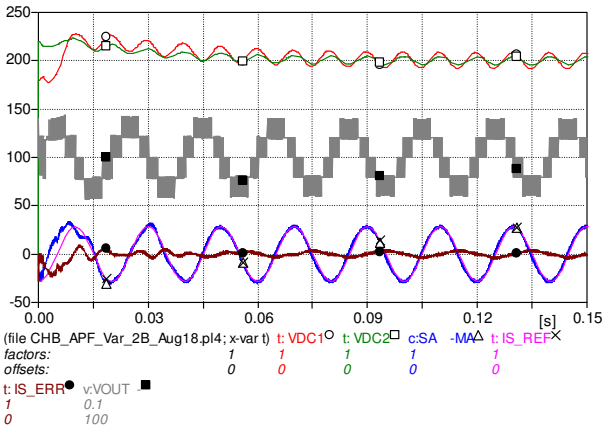


(b)

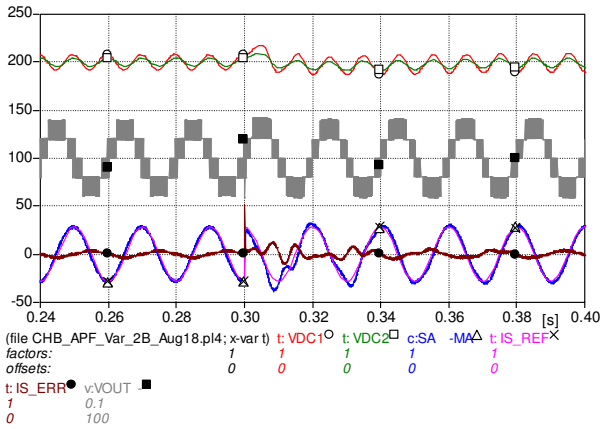
Figure 12. The simulation results of the CHB-DSTATCOM under nominal power-stage parameters. (a) The convergence process after system start-up; (b) Transient response from inductive mode to capactive mode.

Fig.12 shows the time domain simulation results under nominal parameters, where the dc-link voltages, and the synthesized multilevel voltage, grid side current and its reference as well as the tracking error are illustrated. The convergence process after the system start-up is shown in Fig.12(a), where the initial dc-link voltages are set to 180V and 220V, respectively. It can be observed that the dc-link voltages converge to the same value after a few cycles. And the grid-side current tracks its reference value with fast dynamics and the

tracking error approaches zero in the steady state. Fig.12(b) shows the dynamic response of the DSTATCOM when the reference current is undergone a transient change from inductive mode to capacitive mode. It can be observed that the stability of the dc-link voltages is preserved under the transient perturbations. And the grid current tracks its reference within two fundamental cycles, which demonstrates the validity of the control scheme.



(a)



(b)

Figure 13. The simulation results of the CHB-DSTATCOM when Rdc2=100Ω and Cdc2=4000μF. (a) The convergence process after system start-up; (b) Transient response from inductive mode to capacitive mode.

Fig.13 shows the scenario when the resistor and capacitor value of the second inverter are changed as Cdc2=4000μF, Rdc2=100Ω while other parameters remain unchanged. It shows that the stability of the DSTATCOM is ensured and all the waveforms resemble those in Fig.12. However, the dc-link voltage ripple of the second inverter is much less than the first one. And the tracking error of the grid side current is higher in the steady state compared to the case in Fig.12. Besides, a settling time of two cycles under transient perturbation of the reference current can also be observed.

Fig.13 imply that the devised control scheme is quite robustness under power stage parameter variations since the dc-link voltage stability is ensured and the sinusoidal waveform is obtained in the grid side current, with a total harmonic distortion of less than 5% for all these scenarios. It can be inferred that the devised control scheme would produce robust control effect for the CHB-DSTATCOM. Normally, the power-stage parameters deviation is quite small hence a sufficient stability margin can be achieved.

7 CONCLUSIONS

This paper presents an effective control scheme for the cascaded H-bridge (CHB) DSTATCOM. The principle of multilevel carrier-shifted pulse-width modulation (CSPWM) and the mechanism of power balancing among individual H-bridges inverters are presented. The controller synthesis of the CHB-DSTATCOM is provided, which consists of current tracking controller design, the average dc-link voltage controller (AVC) and voltage balancing controller (VBC), which are devised from the devised power balance mechanism. The validity of the devised control scheme is validated by the simulation results from the alternative transient program (ATP/EMTP).

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