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On the Design of Linearly Tunable Wide Input Voltage Range CMOS OTA and Its Application

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Abstract. In this paper, a CMOS OTA with a wide input voltage range and linearly tunable transconductance gain (g_m) is presented. To achieve the linear control of transconductance, the bias current (I_B) is squared by using the current squarer circuit before applying it into the main CMOS OTA. In addition, the source degeneration technique is used to extend the input voltage range. The frequency response of the proposed OTA is analyzed and studied. The performances of the proposed CMOS OTA are tested on PSPICE simulation on TSMC 0.35 µm CMOS technology with a power supply of ±1.5V. The transconductance of OTA can be linearly tuned by adjusting I_B in the range from 1nA to 1.1mA. The proposed OTA also operates well in a wide input voltage range from -1 to 1 volt with a good linearity, and a bandwidth of approximately 8.35 GHz can be achieved. Moreover, a linearly controlled quadrature oscillator based on the proposed CMOS OTA is present to demonstrated the linearly tunable transconductance gain.

Keywords: CMOS OTA, transconductor, linearly tunable, wide input range, quadrature oscillator

Zasnova in uporaba transkonduktančnega operacijskega ojačevalnika s širokim vhodnim napetostnim območjem in linearno nastavljivim ojačenjem

V prispevku je predstavljen operacijski transkonduktančni ojačevalnik OTA v tehnologiji CMOS s širokim vhodnim napetostnim območjem in linearno nastavljivim ojačenjem. Za dosego linearnosti je mirovni tok kvadriran z uporabo tokovnega kvadraturnega vezja pred uporabo v vezju OTA. Zmogljivost vezja, zasnovanega v tehnologiji CMOS TSMC 0.35 µm in napajalno napetostjo ±1.5 V, smo preverili s simulacijami v okolju PSPICE. Analizirali smo tudi frekvenčni odziv vezja. Transkonduktanco vezja OTA linearno nastavljamo s tokom IB v območju od 1 nA do 1.1 mA. Predlagano vezje OTA deluje v območju vhodne napetosti ±1 V z dobro stopnjo linearnosti in pasovno širino 8.35 GHz. Za prikaz in uporabo linearno nastavljive transkonduktance vezja OTA je opisan je tudi kvadraturni oscilator.

1 INTRODUCTION

The operational transconductance amplifier (OTA) is an active building block which functions as a voltage-to-current converter device. It is a fundamental building block of analog circuits especially in signal processing systems and vary useful in many applications such as automatic gain control systems [1], analog multipliers [2], sinusoidal oscillators [3-4], active filters [5] and square-rooters [6]. In many applications, a linearly tunable transconductance controlled by the current or voltage is preferred and most of these designs are constructed from bi-polar transistors which are more complicated and expensive to fabricate than the CMOS trasconductor [7]. However, operation of the CMOS transistors can be expressed as an approximation of a squarer function rather than a linear function. Another disadvantage of the CMOS transconductors [8-9] is their linearly controllable voltage range which is quite limited and not suitable for the low-voltage circuitry due to their weak inversion operating mode.

Due to the advantage of the CMOS technology over the bi-polar technology, many linear CMOS transconductors have been presented [10-12]. Since their transconductance gains are controlled by the DC voltage, the controllable range is limited by the supplied voltage. Therefore, the tunable range is narrow. In a recent approach, current control transconductors have been proposed [13-18], where their g_m can be linearly tuned in a wide range. However, their structures are quite complicated.

Therefore, a new technique to design a wide input voltage range CMOS OTA with a linearly tunable transconductance gain via a DC bias current is presented in this paper. The proposed CMOS OTA is constructed from two parts. The first part is a balanced differential pair with an improved input range by using active resistances at the source of the balanced differential pair in order to reduce the source degeneration, and the second part is a current squarer circuit for the linearly tunable characteristic. The DC bias current of the

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current squarer circuit of the proposed CMOS OTA is not a square-root function so we can linearly tune the transconductance of the proposed circuit. Note that introduction of this technique was presented in our previous work [19]. However, in this paper an extended circuit analysis, frequency-response analysis and circuit performance are presented. In addition, a new linearly tunable quadrature oscillator is proposed to confirm the usefulness of the proposed CMOS OTA. This proposed circuit is verified through the PSPICE simulation based on parameters of the TSMC 0.35μm and an application example of CMOS OTA as a tunable sinusoidal quadrature oscillator is examined and discussed.

2 PRINCIPLE OF OPERATION

2.1. The proposed linearly tunable wide input voltage range CMOS OTA

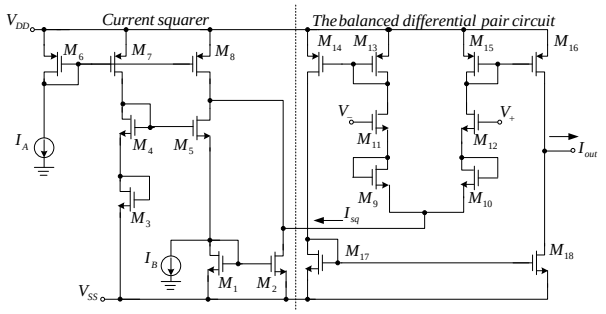

Figure 1. Proposed linearly tunable wide input range CMOS OTA

To obtain a linearly tunable transconductance and a wider input voltage range as compared to the existing CMOS OTA, the proposed CMOS OTA is constructed from two main parts. The first part is a current squarer circuit for the linearly tunable characteristic and the second part is a balanced differential pair with an improved input range by using active resistances at the source of the balanced differential pair in order to reduce the source degeneration. The schematic of the proposed CMOS OTA is shown in Fig. 1. The squarer circuit consists of transistor M1-M8, where M6, M7 and M8 act as current mirrors that provide a bias current for M3, M4 and M5 also M1 and M2 act as a current mirror as well. From a routine circuit analysis, the output current of the squaring circuit (I_{sq}) can be expressed as

$$I_{sq} = 2I_A + \frac{I_B^{\,2}}{8I_A} - I_{D8} \tag{1}$$

If *W/L* of transistor M_8 is set as $(W/L)_{M8} = 2(W/L)_{M6,M7}$, then the output current of the squarer circuit in (1) will be rewritten to

$$I_{sq} = \frac{I_B^{\,2}}{8I_A} \text{ for } |I_B| \le 4I_A \tag{2}$$

where I_A is the bias current of the squarer circuit, and I_B is the DC input current of the squarer circuit.

The wide input range CMOS OTA consists of the current mirrors (M_{13}-M_{14}, M_{15}-M_{16} and M_{17}-M_{18}), differential pair (M_{11} and M_{12}) that is perfectly matched with the source degeneration constructed by the active resistors (M_9 and M_{10}) where I_{sq} is to bias the balanced differential pair. The input voltage of the circuit is determined as

$$V_{in} = V_+ - V_- \tag{3}$$

From the circuit analysis in Fig. 1, input voltage V_{in} in (3) becomes

$$V_{in} = V_{GS12} + V_{GS10} - V_{GS11} - V_{GS9} \tag{4}$$

Since $I_{D11} = I_{D9} = \frac{1}{2}\mu_n C_{ox}\left(W/L\right)(V_{GS11} + V_{th})^2$ and $I_{D12} = I_{D10} = \frac{1}{2}\mu_n C_{ox}\left(W/L\right)(V_{GS12} + V_{th})^2$. Therefore, V_{GS9}, V_{GS10}, V_{GS11} and V_{GS12} are

$V_{GS9} = \sqrt{\frac{2I_{D11}}{\mu_n C_{ox} W/L}} + V_{th9}$, $V_{GS11} = \sqrt{\frac{2I_{D11}}{\mu_n C_{ox} W/L}} + V_{th11}$,

$V_{GS10} = \sqrt{\frac{2I_{D12}}{\mu_n C_{ox} W/L}} + V_{th10}$ and

$V_{GS12} = \sqrt{\frac{2I_{D12}}{\mu_n C_{ox} W/L}} + V_{th12}$, respectively.

By substituting V_{GS9}, V_{GS10}, V_{GS11} and V_{GS12} into Eq. (4), V_{in} can be rewritten as

$$V_{in} = \sqrt{\frac{2}{\mu_n C_{ox}\left(\frac{W}{L}\right)}}\left(2\sqrt{I_{D12}} - 2\sqrt{I_{D11}}\right) \tag{5}$$

By applying KCL to the output node, output current I_{out} can be defined as

$$I_{out} = I_{D16} - I_{D18} \tag{6}$$

and at node I_{sq}

$$I_{sq} = I_{D11} + I_{D12} \tag{7}$$

From Eq. (6), if $I_{D16} = I_{D12}$ and $I_{D18} = I_{D11}$, the drain current will be $I_{D12} = I_{out} + I_{D11}$, by substituting these to Eq. (7), it yields $I_{sq} = 2I_{D11} + I_{out}$. So, currents I_{D11} and I_{D12} can be expressed as

$$I_{D11} = \frac{I_{sq} - I_{out}}{2} \tag{8}$$

and

$$I_{D12} = \frac{I_{sq} + I_{out}}{2} \tag{9}$$

By substituting (8) and (9) into (5), it yields

$$V_{in} = \sqrt{\frac{1}{\mu_n C_{ox} W/L}}\left(2\sqrt{\frac{I_{sq}+I_{out}}{2}} - 2\sqrt{\frac{I_{sq}-I_{out}}{2}}\right) \quad (10)$$

From (10), the output current is obtained as

$$I_{out} = \frac{V_{in}}{2}\sqrt{\mu_n C_{ox}(W/L) I_{sq}} \quad (11)$$

The transconductance gain (g_m) of the balanced wide input range CMOS OTA can be expressed as

$$g_m = \frac{1}{2}\sqrt{\mu_n C_{ox}(W/L) I_{sq}} \quad (12)$$

By substituting I_{sq} in (2) into (12), the transconductance gain can be rewritten as

$$g_m = \frac{I_B}{2}\sqrt{\frac{\mu_n C_{ox}(W/L)}{8 I_A}} \quad (13)$$

If $K=\mu_n C_{ox}(W/L)$, the transconductance gain will become

$$g_m = \frac{I_B}{2}\sqrt{\frac{K}{8 I_A}} \quad (14)$$

From (14), if I_A is fixed, the transconductance gain can be linearly controlled by external DC current I_B. Moreover, it should be noted that the transconductance gain of this proposed CMOS OTA will provide a low-harmonic distortion if the input voltage is limited in the following range

$$-I_B\sqrt{K/4I_A} \le V_{in} \le I_B\sqrt{K/4I_A} \quad (15)$$

2.2. Frequency response analysis of the proposed CMOS OTA

Consider the frequency response of the current-mirror-load-balanced differential pair CMOS OTA. The balanced differential pair CMOS OTA is shown in Fig. 2 with four capacitances, C_m is the total capacitance of the current mirror (M_{13}-M_{14} and M_{15}-M_{16}) at the input node. C_{diff} is the total capacitance of the differential pair and R_L is the total resistor at the output node. The total capacitance of current-mirror C_m can be expressed as

$$C_m = C_{m1} + C_{m2} \quad (16)$$

where C_{m1} and C_{m2} are defined as

$$C_{m1} = C_{gs15} + C_{gs16} \quad (17)$$

$$C_{m2} = C_{gs13} + C_{gs14} \quad (18)$$

The total capacitance of differential pair C_{diff} can be expressed as

$$C_{diff} = C_{diff1} + C_{diff2} \quad (19)$$

where C_{diff1} and C_{diff2} are defined as

$$C_{diff1} = C_{gs12} + C_{gs10} \quad (20)$$

$$C_{diff2} = C_{gs11} + C_{gs9} \quad (21)$$

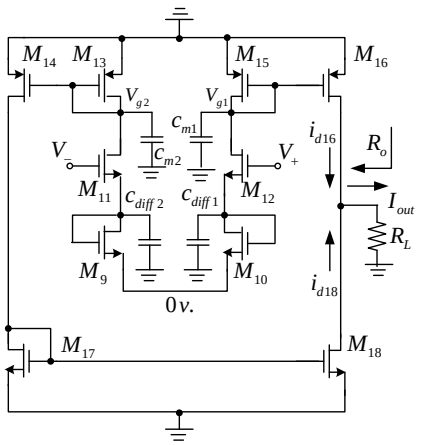

Figure 2. Frequency-response analysis of the circuit in Fig. 1.

As indicated in Fig. 2, transistor M_{12} conducts a drain current signal of $g_m(V_{in}/2)$, which flows through diode-connected transistor M_{15}, and thus through a parallel combination of $1/g_{m15}$ and C_{m2} where we neglect resistances r_{o12} and r_{o15} which are larger than $1/g_{m15}$, voltage V_{g1} can be expressed as

$$V_{g1} = \frac{-\left[g_{m12} - \dfrac{g_{m10}}{g_{m10}+g_{m12}+s\left(C_{gs10}+C_{gs12}\right)}\right]}{g_{m15}+sC_{m1}} \cdot \frac{V_{in}}{2} \quad (22)$$

The drain current of M_{16} can be defined as

$$i_{d16} = -g_{m16} V_{g1} \quad (23)$$

By substituting V_{g1} in (22) into (23), drain current i_{d16} can be rewritten as

$$i_{d16} = \frac{\left[g_{m12} - \dfrac{g_{m10}}{g_{m10}+g_{m12}+s\left(C_{gs10}+C_{gs12}\right)}\right]}{1+\dfrac{sC_{m1}}{g_{m15}}} \cdot \frac{V_{in}}{2} \quad (24)$$

and voltage V_{g2} can be written as

$$V_{g2} = \frac{-\left[g_{m13} - \dfrac{g_{m9}}{g_{m9}+g_{m11}+s\left(C_{gs9}+C_{gs11}\right)}\right]}{g_{m13}+sC_{m2}} \cdot \frac{V_{in}}{2} \quad (25)$$

Since drain current $i_{d14} = i_{d17} = i_{d18}$, i_{d18} is defined as

$$i_{d18} = -g_{m18} V_{g2} \tag{26}$$

By substituting V_{g2} in (25) into (26), drain current i_{d18} can be expressed as

$$i_{d18} = \frac{\left[g_{m11} - \dfrac{g_{m9}}{g_{m9} + g_{m11} + s\left(C_{gs9} + C_{gs11}\right)} \right]}{1 + \dfrac{sC_{m2}}{g_{m13}}} \cdot \frac{V_{in}}{2} \tag{27}$$

Now, at the output node, the total current is

$$i_{out} = i_{d16} + i_{d18} \tag{28}$$

which flows though a parallel combination of $R_o = r_{o16} // r_{o18}$ and R_L, thus

$$V_o = i_{out} \frac{1}{\dfrac{1}{R_o} + R_L} \tag{29}$$

By substituting i_{out} in (28) into (29), where $g_{m9} = g_{m10} = g_{mR}$, $g_{m13} = g_{m15} = g_{m_{cm}}$ and $g_{m11} = g_{m12} = g_{m_{diff}}$. The voltage transfer gain is written as

$$\frac{v_o}{v_{in}} = \frac{g_{m_{diff}} - \dfrac{\dfrac{g_{m_R}}{g_{m_R} + g_{m_{diff}}}}{1 + \dfrac{sC_{diff}}{g_{m_R} + g_{m_{diff}}}}}{1 + \dfrac{sC_m}{g_{m_{cm}}}} \cdot \left[\frac{1}{\dfrac{1}{R_o} + R_L} \right] \tag{30}$$

Eq. (30) indicates that capacitance C_m at the input of the current mirror gives rise to a pole with frequency f_p

$$f_p = \frac{g_{m_{cm}}}{sC_m} \tag{31}$$

and a zero with frequency f_z

$$f_z = \frac{g_{m_R} + g_{m_{diff}}}{sC_{diff}} \tag{32}$$

Eq. (32) indicates that capacitance C_{diff} at the differential pair gives rise to a zero with frequency f_z.

2.3 Application example: A linearly tunable sinusoidal quadrature oscillator

The quadrature oscillator is a typical sinusoidal oscillator which provides two sinusoidal outputs with a 90 degree phase shift. It is found useful in measurement systems, simple sideband generators, quadrature mixers, vector generators and selective voltmeters [20-22]. In order to demonstrate the advantage of the proposed tunable CMOS OTA, a quadrature oscillator based on the proposed CMOS OTA oscillation frequency which can be linearly controlled is presented. Fig. 3 shows a block diagram of the quadrature oscillator which is composed of an integrator circuit, amplifier circuit and adder/subtractor circuit.

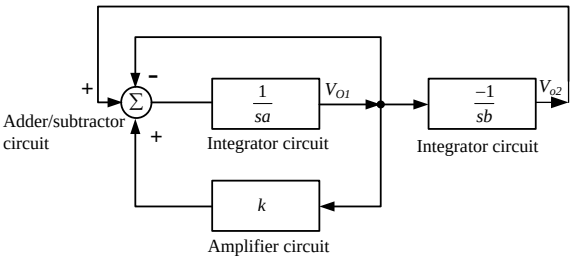

Figure 3. Block diagram of the quadrature oscillator

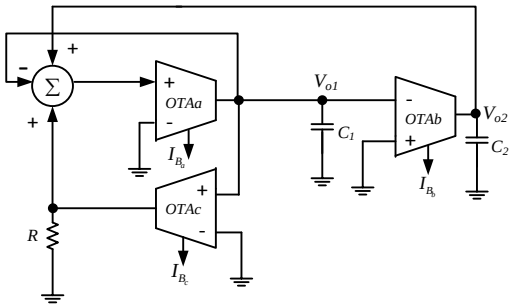

Figure 4. Schematic diagram of the quadrature oscillator

Based on the block diagram in Fig. 3, the oscillator consists of three CMOS OTAs, two grounded capacitors, one adder/subtractor circuit and one resistor. A schematic diagram of the circuit is shown in Fig. 4, where OTA_a and C_1 function as integrator a, OTA_b and C_2 function as integrator b and OTA_c is the amplifier circuit. The characteristic equation of the circuit can be obtained as

$$s^2 C_1 C_2 + sC_2 g_{m_a}\left(1 - g_{m_c} R\right) + g_{m_a} g_{m_b} = 0 \tag{33}$$

From (33), the condition of oscillation and frequency of oscillation are written as

$$R g_{m_c} \geq 1 \tag{34}$$

and

$$\omega_{osc} = \sqrt{\frac{g_{m_a} g_{m_b}}{C_1 C_2}} \tag{35}$$

From (34) and (35), if $g_{m_a} = \frac{I_{B_a}}{2}\sqrt{\frac{k}{8I_A}}$, $g_{m_b} = \frac{I_{B_b}}{2}\sqrt{\frac{k}{8I_A}}$ and $g_{m_c} = \frac{I_{B_c}}{2}\sqrt{\frac{k}{8I_A}}$, it yields

$$\frac{RI_{B_c}}{2}\sqrt{\frac{k}{8I_A}} \geq 1 \tag{36}$$

and

$$\omega_{osc} = \sqrt{\frac{I_{Ba}I_{Bb}k}{32I_AC_1C_2}} \tag{37}$$

If I_{Ba}=I_{Bb}=I_B, Eq. (37) can be reduced to

$$\omega_{osc} = I_B\sqrt{\frac{k}{32I_AC_1C_2}} \tag{38}$$

From (38), the frequency of oscillation can be linearly tuned with I_B while the condition of oscillation can be adjusted by I_{Bc}. From (36) and (38), it is obvious that the condition of oscillation and frequency of oscillation can be adjusted independently. The relationship between output voltages V_{o_1} and V_{o_2} can be expressed in the voltage transfer function as

$$\frac{V_{o_2}(s)}{V_{o_1}(s)} = \frac{-g_{m_b}}{sC_2} \tag{39}$$

The voltage of the sinusoidal steady-state can be rewritten as

$$\frac{V_{o_2}(j\omega)}{V_{o_1}(j\omega)} = \frac{-g_{m_b}}{\omega C_2}e^{j90^o} \tag{40}$$

It is found from (40) that the quadrature output voltage, (V_{o_1} and V_{o_2}), has the phase difference at 90°.

3 Simulation Results

PSPICE was used to verify the performances of the proposed CMOS OTA. The technology used in the simulation was the TSMC 0.35µm n-well CMOS process. The parameters of the MOS transistors were in level 3. The dimensions of the MOS transistors are illustrated in Table 1. The power supply voltages were set at V_{DD} = -V_{SS} = 1.5 V and bias current I_A was set at 200µA.

Table 1. Dimensions of the CMOS transistors.

MOS transistors	W(µm) / L(µm)
M1-M7, M11-M18	1.75/0.35
M8	3.5/0.35
M9, M10	0.35/0.35

Fig. 5 shows the simulation result of the output current (I_{out}) versus the input voltage (V_{in}) when the bias current (I_B) was set at 500µA, 700µA and 800µA, respectively. It clearly shows that in case of I_B at 500µA, 700µA and 800µA, the input voltage is linearly converted to be the output current with a nonlinearity of less than 2.5% for the input voltage(V_{in}) in the range from -0.8 to 0.8V, from -0.97 to 0.97V and from -1.01 to 1.01V, respectively. These results were agreed with (15). g_m, when the DC bias current I_A=200µA and the DC bias current I_B=500µA, was 0.38mA/V.

The plot of the relationship between g_m and the input voltage in the range from -1.1 to 1.1V is shown in Fig. 6. It shows that, in the case of I_B = 500µA,700µA and 800µA, the circuit can linearly convert the input voltage into the output current for V_{in} in the range from -0.7 to 0.7V, from -0.8 to 0.8V and from -0.6 to 0.6V, respectively, with the transconductance nonlinearity of less than 3%.

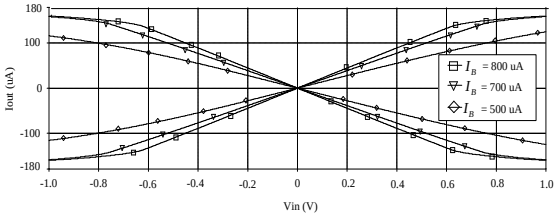

Figure 5. DC transfer characteristic of the proposed CMOS OTA

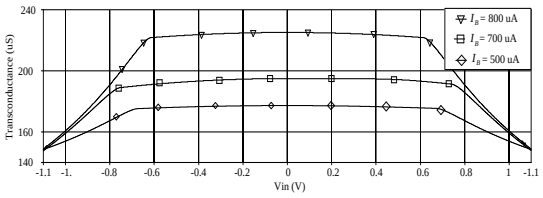

Figure 6. Transconductances versus the input voltage

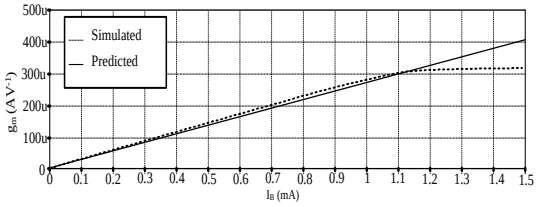

Figure 7. Linear transconductance tunable range

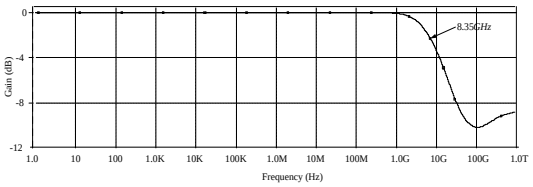

Figure 8. Frequency response of CMOS OTA

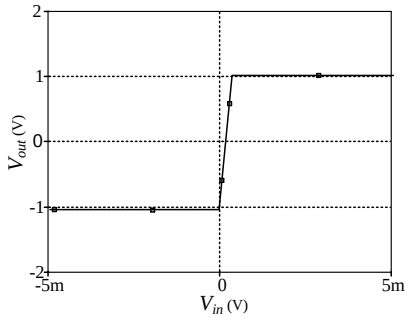

Figure 9. Simulation result of the input offset voltage of the proposed CMOS OTA

Fig. 7 shows the plot of the relationship between transconductance gain g_m and DC bias current I_B. It was measured by setting I_A=200µA and varying I_B from 1nA to 1.2mA. This result shows that g_m can be linearly tuned by bias current I_B over the current range from 1nA to 1.1mA, where the simulated conversion error is less than 4.3%. The frequency response of the proposed circuit is shown in Fig. 8, in the case of the DC bias current I_B=500µA, transconductance gain g_m=3.8×10^{-4}V/A, g_{m_B} =1.7×10^{-4}V/A, $g_{m_{cm}}$ =3.8×10^{-4}V/A, C_m =1.81×10^{-15}F and C_{diff} =3.8×10^{-15}F, a -3dB bandwidth of approximately 8.35 GHz is achieved. From this result it is found that the frequency response of the proposed CMOS OTA is according to calculation (22) with an error of about 5%. Fig. 9 shows the input offset voltage of a linear wide input range CMOS OTA by setting the bias currents $I_B = 700\mu A$, and input voltage V_{in} is varied from $-5mV$ to $5mV$, the input offset voltage is $|V_{OS}| = 0.24mV$ where R_L=1kΩ and the output voltage (V_{out}) is measured from the voltage dropped on R_L. The characteristic of the linear wide input range CMOS OTA is shown in Table 2.

Table 2. Performance data of CMOS OTA.

Parameters	Values
Power supply voltage	±1.5V
Power consumption	3.05mW
3dB bandwidth	8.35GH$_z$
Input voltage range	-1.01V to 1.01V
Bias current (I_B) range for linear g_m	1nA to 1.1mA
Offset voltage	0.24mV
Gain margin	-95.22dB
Phase margin	90.09^o

The performances of the proposed linearly tunable quadrature oscillator in Fig. 4 were verified through a PSPICE simulation. For the design on PSPICE, the frequency of oscillation (f_{osc}) was 600kHz. The bias currents of OTA$_a$ and OTA$_b$ were set at 500 μA ($I_{B_a} = I_{B_b} = I_B = 500\mu A$) and the bias current of OTA$_c$ was set at $697\mu A$ ($I_{B_c} = 697\mu A$) and $C_1 = C_2 = 50pF$.

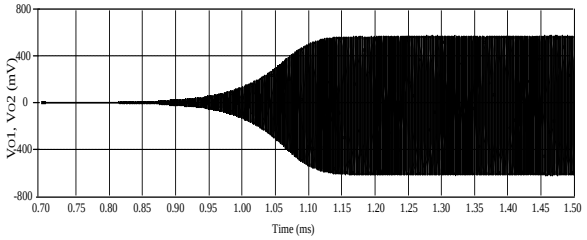

Figure 10. Output waveform at the initial state

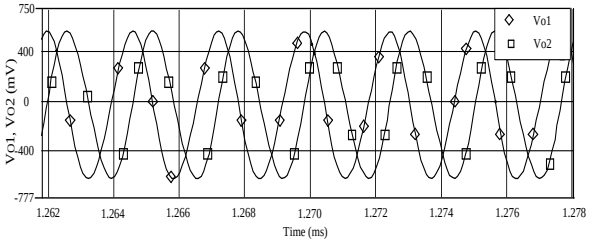

Figure 11. Output waveform at a steady-state

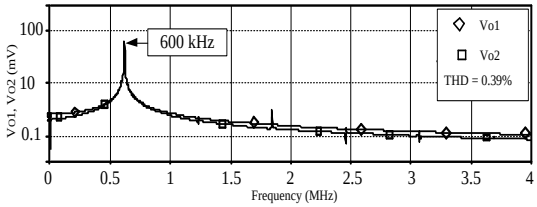

Figure 12. Output waveform at a steady-state

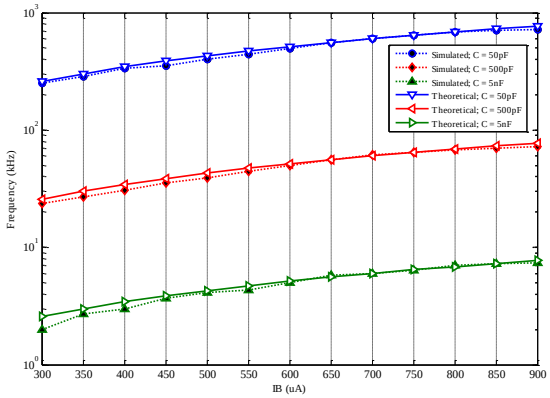

Figure 13. Output frequency versus the I_B current

From the condition of (36), the resistor (R) will be equal to 5.2kΩ. Figs. 10 and 11 show the output waveform at the initial state and the output waveform at a steady-state of V_{o1} and V_{o2}, respectively. Fig. 12 shows the output spectrum of the quadrature oscillator where the simulated oscillation frequency was obtained at 600 kHz, and the total harmonic distortion (THD) was approximately 0.39 %. Fig. 13 shows the plots of the simulated and theoretical oscillation frequencies versus bias currents I_B where C_1 and C_2 with identical values are 5nF, 500pF and 50pF. It is seen that the simulation results are in accordance with the theoretical analysis shown in (38).

4 CONCLUSION

In this paper, a new design of the linearly tunable transconductance gain and wide input voltage range CMOS OTA is presented. In order to obtain a linear gain adjustment and a wider input voltage range, the proposed CMOS OTA is constructed with an improved balanced differential pair and the current squarer circuit. This enables the proposed OTA to achieve a linear controllability of the tranconductance gain with a nonlinear transconductance of less than 4.3%. Moreover, a wider input voltage range from -1.1V to 1.1V is obtained. The PSPICE simulation with the TSMC 0.35 μm CMOS technology can demonstrate the performance of the proposed CMOS OTA. The operating frequency response of the proposed CMOSOTA can be up to appoximately 8.35GHz with the power consumptions of 3.05mW. In addition, the simulation results of the proposed quadrature oscillator were obtained to verify the theoretical analysis.

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